EPCI
European Passive Components Institute

EEE PASSIVES SEMINAR: TRENDS AND AI IMPACT

ESA SPCD 2026 Space Passive Component Days | ESA/ESTEC, 13 October 2026, 14:00–16:00

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Seminar Roadmap: Two Parts, Two Hours

ESA SPCD 2026 pre-conference seminar | ESA/ESTEC Noordwijk | Tuesday 13 October 2026, 14:00–16:00

PART 1 | 14:00–14:50

Introduction 14:00 - 14:15

The Changing Landscape

Structural trends, market size and sentiment, supply chain, and technology shifts in capacitors, resistors, inductors and circuit protection.

BREAK | 14:50–15:10

20 Minutes

Coffee and networking. Questions from Part 1 can be collected for the discussion at the end.

PART 2 | 15:10–16:00

AI Cloud & Physical AI

How AI data-centre and physical-AI hardware transform passives, and how that carries into autonomous, flying, dual-use and space systems.

Thread through both parts: what the commercial upcycle and the AI hardware wave mean for current and future passive components technology development and its potential impact to space programmes

Introduction

ESA SPCD 2026 pre-conference seminar | ESA/ESTEC Noordwijk | Tuesday 13 October 2026, 14:00–16:00

Speaker

- Electrotechnology Degree by Technical University of Brno,Czech Republic in 1993
- Ph.D. in Tantalum Capacitors in 2000> 21 years working for tantalum capacitor manufacturer
- > 15 years in position of Worldwide Technical Marketing Manager at KYOCERA AVX
- more than 70 technical papers and 1 US/international patent, 4 outstanding/best award technical papers at CARTS passive component conference
- 2005 Dr. Zandman award for a great contribution to passive component industry
- Lecturer of capacitor technologies, presentation skills and inter-culture communication
- July 2015 – Founder of the European Passive Components Institute
- Founder of Passive Components Blog www.passive-components.eu the largest blog globally dedicated to passive components
- Since 2017 organizer of **PCNS** bi-annual Passive Components Networking Symposiums



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Introduction

Passive Components Blog

be active with passives!

since 2015

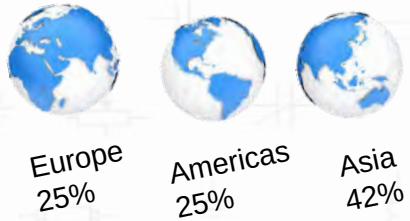
ESA SPCD 2026 pre-conference seminar | ESA/ESTEC Noordwijk | Tuesday 13 October 2026, 14:00–16:00

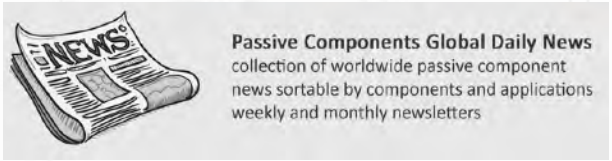
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| **No.1** Global Passive Components Educational & Information Blog

Website profile:

Active visitors: ~**60K-90K/month**
Google Search views: ~ **2.5 million views /month**
Google Search clicks: ~ **13 thousands clicks / month**
Newsletter: > **892** subscribers related to passive components
Top countries: USA, India, Germany, UK, Canada, France, Sweden





WHO is WHO in Passives
free online database of global passive components manufacturers & suppliers



EPCI members and supporters

- **One of few educational and information resources dedicated solely to passive components**
- EPCI among the **top best-rated global component blogs**
- **PCNS Passives Symposium** organizer since 2017
- Covers a broad passive-components **industry ecosystem**
- Publishes timely **industry updates**, including capacitors, inductors, resistors, EMI/EMC, modelling, and market & supply chain topics
- Highlights **application trends** such as AI data centers, automotive electronics, EV power systems, RF, and industrial design
- Combines product news with **deeper engineering content**, including converter design, MLCC technology, inductor modelling, and technical calculation articles
- Supports **professional engagement** through upcoming events, webinars, archives, newsletter subscription, and supplier visibility

Dossiers

Home | News | Knowledge Blog | Dossiers | Suppliers | PCNS | Events

Technology Dossiers for Design, Sourcing and Strategy Teams

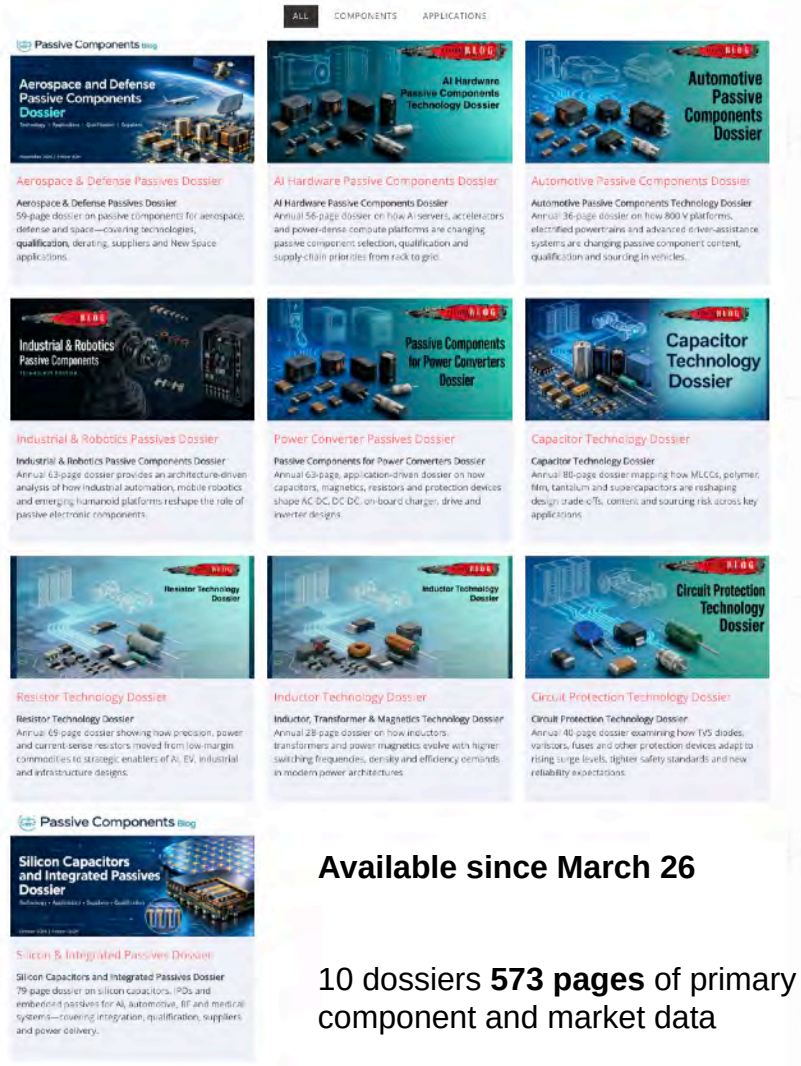
- Passive Components Blog prime source

Annual technical dossiers combining market data, technology benchmarking and application guidance across passive components, AI hardware, automotive and power conversion.

“Where is the passive component device industry heading over the next 5–10 years?”

“Which technologies and applications define the strategic roadmap at present stage?”

- in-depth, year-in-review latest trends and news
- market data, vendor roadmaps, standards updates, application case studies
- scope: 60–90 pages typically covering global market outlook, technology roadmap, standards and compliance, key applications, and supply-chain evolution.
- purpose: Long-horizon planning for engineering, sourcing, and product strategy teams
- positioning: A curated “yearbook” for the component technology and markets, built on the most relevant market studies and vendor publication.



Available since March 26

10 dossiers **573 pages** of primary component and market data

PART 1

14:15 – 14:50

The Changing Landscape of Passive Components

01 Structural forces

02 Market size and sentiment

03 Supply chain, pricing and materials

04 Capacitor technologies

05 Resistors, inductors, protection

06 Qualification and space implications

07 Key Growth Areas

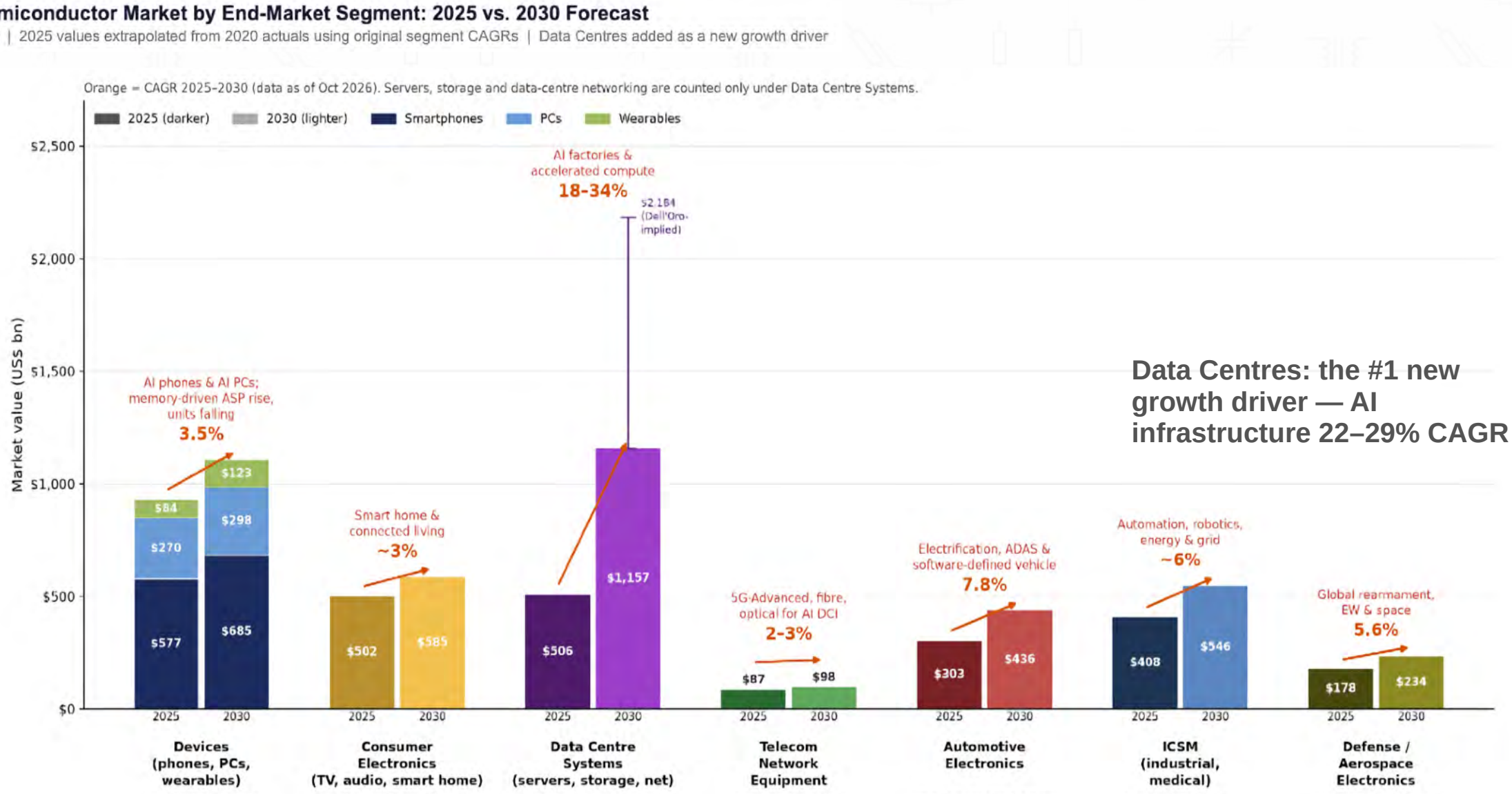
Seminar Objectives

What attendees should take away by 16:00

1. **Latest trends** in EEE passives — capacitors, resistors, inductors and circuit protection — tailored to application requirements.
2. **Emerging technologies and supply dynamics** that are reshaping availability, and qualification.
3. **AI hardware requirements** and how they transform passives for autonomous systems such as flying and dual-use platforms.
4. **Broader impact of cloud and physical AI** on EEE applications, incl. space sectors.

Source: ESA SPCD 2026 programme announcement

Mega Trends in Electronics for the Rest of the Decade and Beyond



Data Centres: the #1 new growth driver — AI infrastructure 22–29% CAGR

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Six Forces Reshaping Passive Components

1 AI power delivery is the demand engine — and it is a passives problem, not a silicon problem.

2 Voltage escalation 12 V → 48 V → 400 V → 800 V DC recurs across automotive, industrial, aviation and data centre.

3 Wide-bandgap switching relocates loss, EMI and risk out of the semiconductor and into the passive.

4 Parasitics over value ESL, DCR and mounting inductance — not C or L — are the binding parameters.

5 Integration moves passives into the package, the module and the die.

6 Qualification as a moat AEC-Q200, MIL and ESCC routes and multi-year line qualification decide market access.

THE STRUCTURAL SHIFT

Passives moved from the last line of the BOM to the first constraint on system performance.

In AI server platforms, passive components now sit in a bill-of-materials cost position second only to GPUs and memory.

Source: EPCI Technology Dossiers 2026

From Invisible Commodity to Design Parameter

2026 is a segmented, K-shaped market — not the broad allocation of 2018

2018 ALLOCATION

Broad

Shortages and extended lead times across a wide range of voltage classes, case sizes and application segments.

2026 UPCYCLE

K-shaped

High-end AI and automotive MLCC tight and expensive; many commodity grades closer to balance.

DURATION

Into 2027/2028

Constraints in high-grade MLCC may persist into 2027/2028 as AI power subsystems take a rising share of premium capacitance.

Stressed categories: high-capacitance MLCC, selected automotive MLCC series, high-frequency MLCC, high-Q inductors and certain magnetics.

Commercial Design-in rule: qualify at least two manufacturers or technologies for critical positions such as key MLCC nodes on power rails.

Source: Passive Components in 2026: Commodity to Design Parameter | MLCCs in the Age of AI: Q2 2026

End Market and Electronic Components Trends

Auto

Industrial

Smartphones/CE

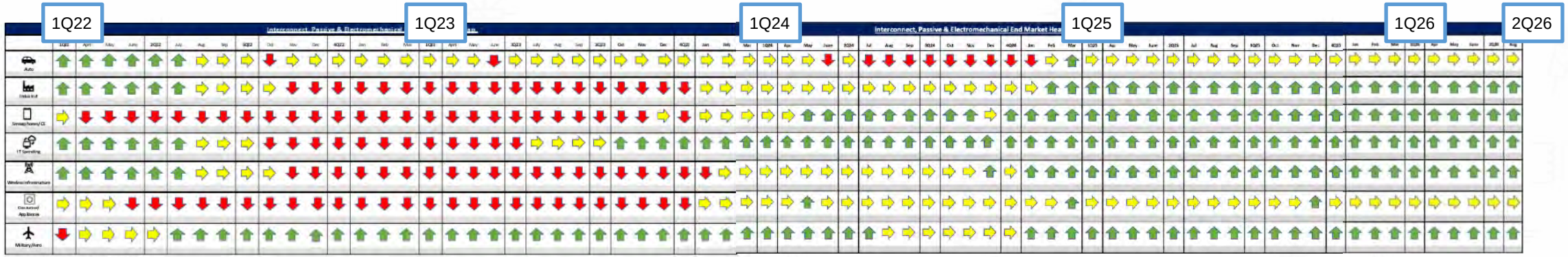
IT Spending

Wireless Infrastructure

Consumer/ Appliances

Military/Aero

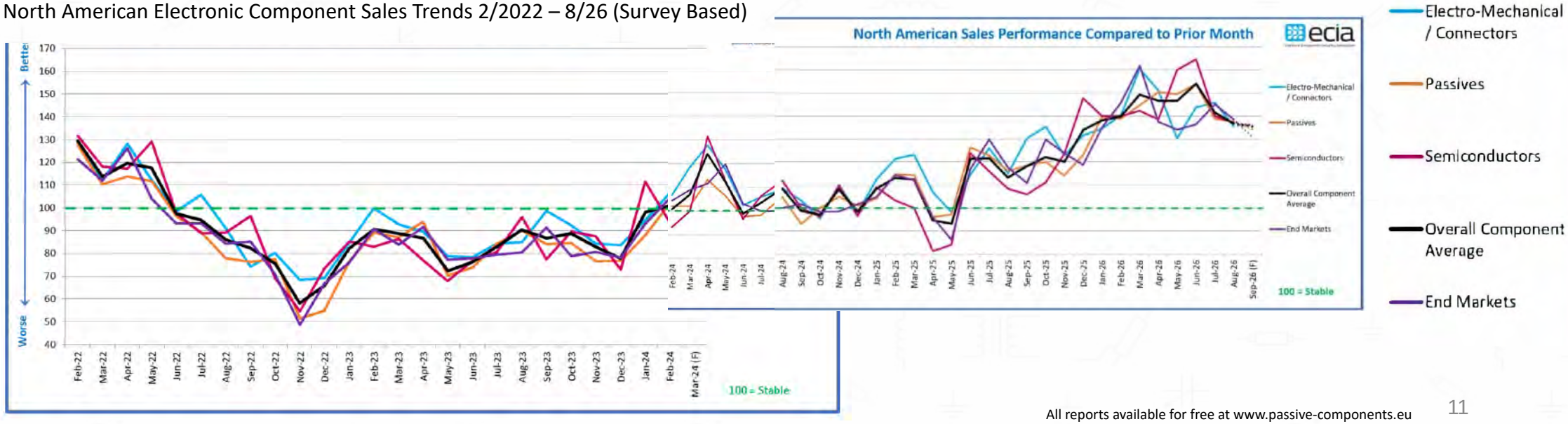
End Electronic Market Trends 2/2022 – 8/2026



Source: Edgewater Research

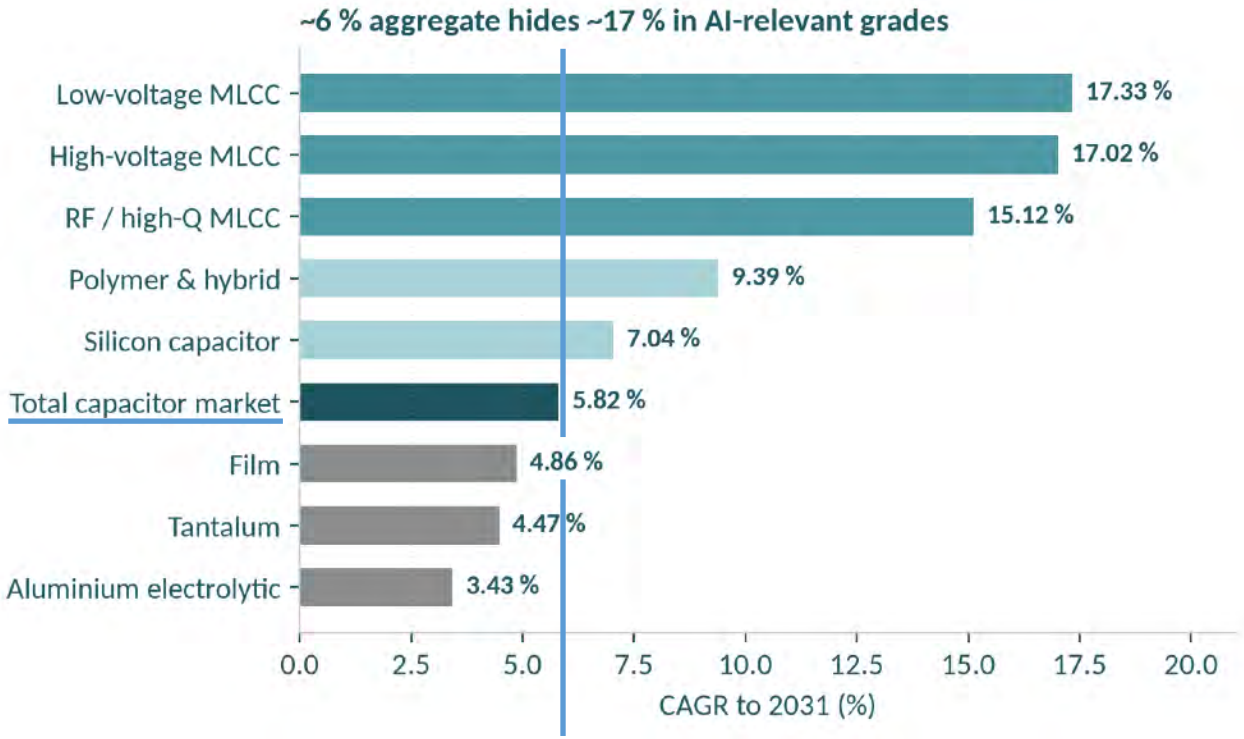
** Green Arrow represents strong/improving demand; Yellow - stable/mix demand; Red - weak/declining*

North American Electronic Component Sales Trends 2/2022 – 8/26 (Survey Based)



Aggregate Growth Hides a Re-Weighting - Capacitors

Segment CAGRs to 2031 range from 3.4 % to 17.3 % inside the same capacitor heading



READING THE SPREAD

Two markets that share one tariff heading

AI-grade low-voltage MLCC: USD 18.97 bn in 2026, 17.33 % CAGR to USD 42.18 bn in 2031 — a separate universe, never added to totals.

High-voltage MLCC: USD 5.64 bn at 17.02 %. Silicon capacitors: USD 2.30 bn at 7.04 %.

Aluminium wet electrolytic: USD 4.63 bn at 3.43 % — the slow end of the distribution. Polymer and hybrid aluminium capacitors types taking the share and growth.

Tantalum MnO2 capacitors growth limited, market is moving to polymer types.

Source: EPCI Capacitors Technology Dossier 9/26

Bookings Outrun Inventory Normalization

Interconnect, passive and electromechanical demand into 2027



2026 Connector Growth

Book-to-bill > 1x for the broader IP&E segment in July; one channel source reported B2B above 1.3x with lean inventories.

MLCC and resistor orders accelerated sharply from June, led by Greater China; capacity mix is concentrated on larger AI case sizes.

AI rack signal suppliers are reportedly asked to prepare for more than 100K NVL72 racks in 2027.

Defense elevated defense spending is named as a driver of the USD 34.3 bn connector backlog at June 2026.

Risk optical-component availability and Rubin Ultra density could shift timing and content allocation.

Source: August 2026 Market Insights | Connector Industry Performance mid-2026

Passive Component Lead Times

8–20+ WEEKS — **Commodity SMD MLCC**
Broad supply remains manageable

20–40 WEEKS — **AI/HPC high-cap MLCC**
Selective high-density constraint

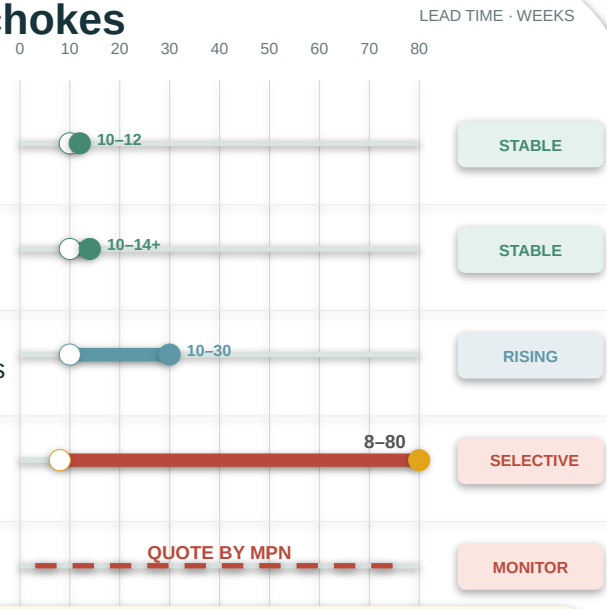
8–80 WEEKS — **SMD power inductors**
Highly segmented by construction

Capacitors & resistors



Interpretation: AI pressure is concentrated in compact high-capacitance parts with strong DC-bias performance; “high-CV” alone is not a complete AI-risk definition.

Inductors & chokes



Power magnetics are bifurcated

Ordinary catalog parts are broadly stable. TLVR, coupled and high-current low-DCR parts require platform- and MPN-level confirmation.

! Procurement implication

One lead time can not be applied to all MLCCs or inductors: screen AI/HPC capacitance-density and high-current magnetics by exact MPN, qualification and supplier allocation.

Sources: Avnet Abacus Lead-Time Guide (Aug 2026); ETNews (17 Aug 2026); TDK TLVR application note (2 Apr 2026). Ranges are supplier/MPN dependent. HPC=High Performance Computing

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Concentration and Supply Chain Bottlenecks

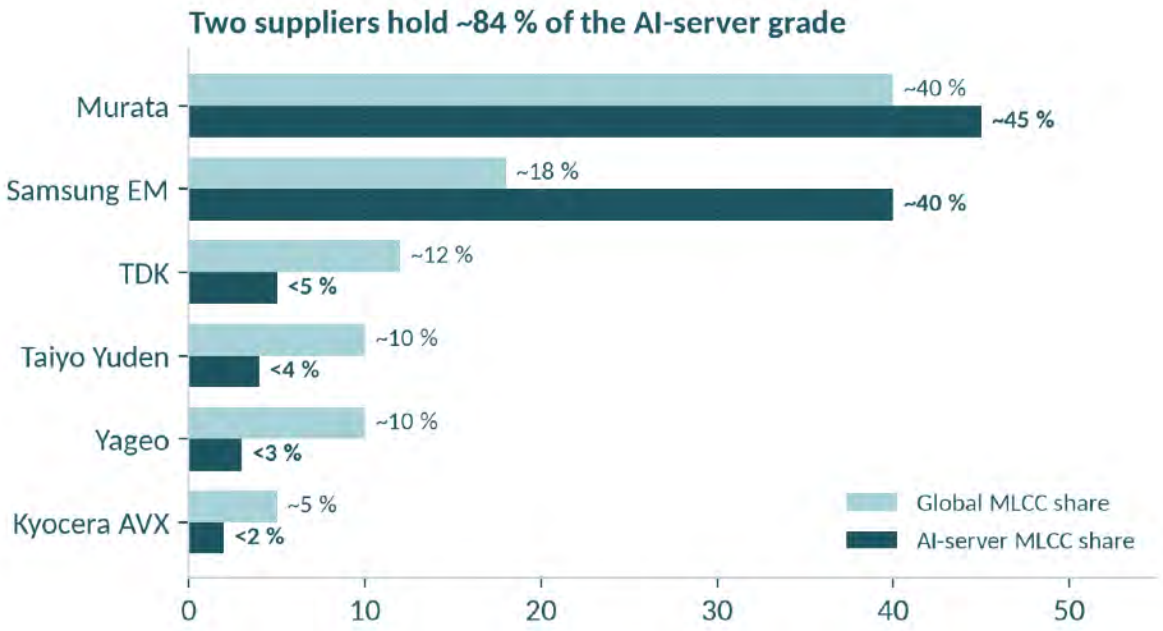
Capacity pre-selling means the 2026–2028 supply position is already largely fixed

Dimension	Position	Implication
AI-server MLCC	Murata + Samsung EM ≈ 84 % of supply	Effective duopoly on the critical grade
Ferrite	China ≈ 70 % of global capacity	Single-region magnetic core dependency
Resistor production	APAC ≈ 71 %; Western cost 35–50 % higher	Reshoring carries a structural cost penalty
Thin-film IPD	Only 8 of 30 makers can build sophisticated IPDs	Integration capability is scarce
Capacitor film	One supplier consistently produces the <3 µm grades	Risk sits in the film, not the winding
Capacity pre-selling	KRW 1.82 tn of 2026 MLCC contracts; KRW 1.5 tn silicon capacitor contract	2027–2028 capacity already locked out
Pricing	MLCC X5R +15–25 % (June 2026); one supplier ~+50 % list from 1 July 2026	Price is no longer the lever

Concentration Rises With Grade

MLCC

No third supplier could absorb redirected AI-grade demand



Segment	Concentration
AI-server MLCC	Murata + Samsung EM ≈ 84 %
Top-5 MLCC (global)	≈ 77 % of market
Tantalum	KEMET, Panasonic, Kyocera AVX, Vishay in total 60–70 %
High-voltage MLCC	Top-5 ≈ 70 % of capacity
Aluminium electrolytic	Top-5 ≈ 40 % — most fragmented
Ferrite capacity	China ≈ 70 %
Sub-3 µm BOPP film	Very few plants

Source: EPCI Capacitors Technology Dossier 9/26 | MLCCs in the Age of AI: Q2 2026 | EPCI Technology Dossiers 2026

Geography and Geopolitics Rebuild Supply - MLCC

China rises in volume; high-end ceramic remains Japanese and Korean

CHINA MLCC SHARE

6 → 10 %

2019 to 2024, forecast 15–20 % by 2030.

HIGH-END SELF-SUFFICIENCY

< 20 %

China, computing and automotive MLCC.

DIELECTRIC GAP

< 0.5 µm vs ~1 µm

Japan/Korea >1,500 layers vs ~1,000 layers.

MURATA CHINA REVENUE

60 → < 50 %

2021 to the latest fiscal year.

SUPPLY-CHAIN DECOUPLING

Rare earths and dual supply chains

Murata plans separate rare-earth supply chains for the US and China over about three years, auditing non-Chinese mining and refining routes.

Full replacement of Chinese-origin rare earths may not be technically or economically feasible near term.

Source: EPCI Capacitors Technology Dossier 9/26 | Murata to Decouple China Rare Earth Supply | Wk 36 Supply Chain Digest

Raw Material Pricing Trends

Metal	6M Signal	Passive-Component Exposure
Copper	+21.3%	Broadest cost exposure: leadframes, foils, wire and terminations.
Aluminum	+3.0%	Aluminum-electrolytic foils, cans and housings; volatility still matters.
Silver	-5.3%	Conductive pastes and thick-film terminations; level remains expensive.
Gold	-2.8%	Plating and specialty terminations; smaller volume, high unit-value impact.
Ruthenium	Elevated	High-value thick-film resistor pastes; tight spot availability is the risk.
Tantalum	Supplier check	Capacitor-grade powder and wire; monitor regional premiums and lead times.
Nickel / PGMs	Mixed	Nickel electrodes/alloys; Pt/Pd mainly legacy and specialty applications.

6-Month Signal & Component Exposure

Market snapshot

17 September 2026

COPPER	ALUMINUM
$6.66/lb	$3,454/t
+21.3% · 6M	+3.0% · 6M

SILVER	GOLD
$66.52/oz	$4,411/oz
–5.3% · 6M	–2.8% · 6M

Tantalum Capacitors

High Risk Exposure

Direct cost transmission from +60% metal price surge.

Power Magnetics

High Cost Baseline

Wiring and broad component cost impact by copper +21%

Thick-Film Resistors

Elevated Cost Baseline

Pressured by Silver pastes and Ruthenium price increases.

MLCCs & Terminations

Moderate Impact

Silver price multi-year highs

Aluminum Electrolytics

Volatile Baseline

Foils and cans subject to ongoing aluminum price swings.

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Metal Prices Became a Design Constraint

Silver, tantalum, aluminium foil and palladium drive the 2026 cost base

SILVER

> 70 USD/oz

NYMEX futures; silver paste can exceed 50 % of the production cost of some ferrite-bead types.

TANTALUM

x2.6

Ingot RMB 2,600/kg (end 2025) to RMB 6,650/kg (11 Aug 2026); Europe metal +60 % early 2026.

ALUMINIUM CHAIN

+30–40 %

Chemical materials for aluminium electrolytics; metal prices about +10 %; foil lead times doubled.

THICK FILM / VARISTORS

+10–30 %

Chinese makers: varistors and ceramic caps +10–20 %, thick-film circuits +15–30 %.

SUPPLIER RESPONSE

Thinner or alternative finishes, base-metal electrodes and material optimisation to cut silver, palladium and gold exposure — construction changes that space users must track through change notifications.

Source: How Metal Prices Drive Passive Price Hikes | EPCI Capacitors Technology Dossier 9/26 | AI Data Centers Push Aluminium Capacitor Prices

Capacity Reallocation Is an Obsolescence Risk

Long-lifecycle programmes compete with AI lines for the same plants

Reallocation

Murata and Samsung EM are shifting capacity toward higher-value AI MLCC lines, constraining conventional lower-capacitance output.

End-of-life

Selected specifications across nine Murata MLCC series reportedly received EOL notices — general-purpose, automotive and RF.

Construction drift

Metal thrifting and new electrode systems change parts that carry the same family name.

COUNTER-MOVES IN THE HI-REL BASE

Exxelia promotes a long-term no-obsolescence policy with European and US manufacturing; Evans Group unified four US hi-rel capacitor makers under one interface.

Source: YAGEO July 2026 price increase | Samsung MLCC outlook | Exxelia 1200 V for 800 V aerospace | Evans Group

Capacitor Technology Map 2026

Where each family is moving — and what is pulling it

Family	2026 direction	Primary driver	Space relevance
Class II MLCC	47–330 µF X6S at 2.5–4 V; < 0.5 µm layers	AI accelerator PDN	Bridge hi-rel grades, derating
Class I / HV MLCC	C0G to 3 kV, 150 °C stacked parts	800 V AI and EV power	Resonant, snubber, EMI
Polymer tantalum	Low ESR at 2.5–75 V; 150 °C automotive	AI servers, automotive	COTS-plus for LEO
Aluminium / hybrid	High-ripple, long-life; solid Al vs Ta	Data-centre PSUs	Bulk and hold-up
Film	1,200 V on 800 V buses; 125–140 °C PP	SiC traction, aviation	HV converters, PPU
Silicon	Trench 220–542 nF/mm²; into package	Interposer, land side	Rad-hard, −250…+300 °C
Supercapacitor	3,500 A pulses; UL 810A	AI load smoothing	Launcher and spacecraft peaks

Source: EPCI Capacitors Technology Dossier 9/26 | C0G HV MLCC for 800 V AI | Skeleton 3500 A supercapacitor | Polymer tantalum for LEO

MLCC Development Background

Boost in Demand for MLCC and its Development

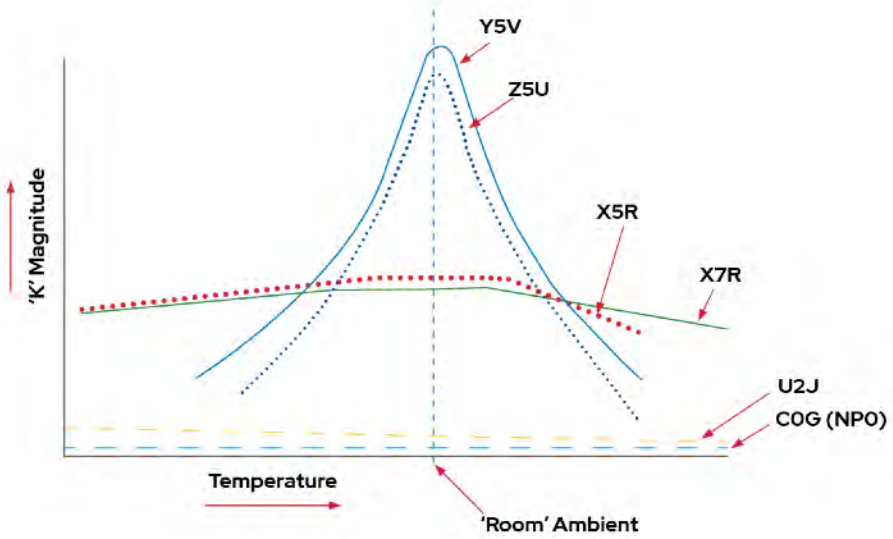
Demand for MLCC capacitors in servers to quadruple by 2029

Demand for AI servers and other IT infrastructure applications will grow as cloud AI becomes more prevalent

Servers (Baseboard)*	1,800–2,500
AI servers (Baseboard + AI accelerators × 8)*	**10,000–20,000**

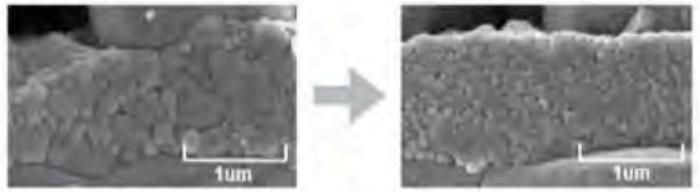
- High reliability
- Increased capacity

- Fine grained ceramic dielectric materials
- Uniform dispersion / purity
- Thinner layers
- New dielectric materials

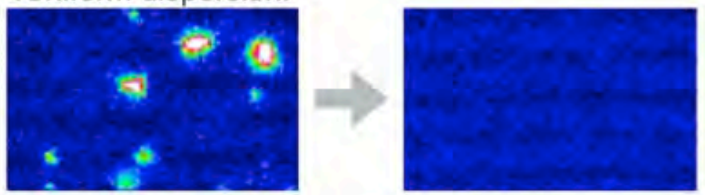


miniaturization and higher capacity technologies

<Fine grained ceramics>



<Uniform dispersion>



<Thinning of electrode and dielectric>



High capacitance MLCC roadmap (6.3V rated or less)



Growth potential in the AI【Edge devices】

Because of the high computational power requirements, the power needed for semiconductors is expected to increase, leading to a further rise in demand for miniaturization and high-capacity solutions due to space constraints on edge devices.

source: Samsung Electro-Mechanics, Murata

Film vs MLCC Capacitor Technology - 800 V Application

Class I ceramic and polypropylene film for wide-bandgap power stages

Film Capacitors



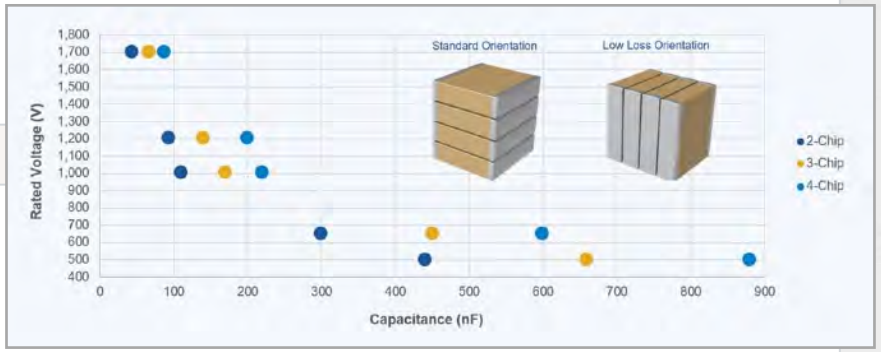
Class I vs Class II dielectric: C0G / NP0 Class I - Stability

±30 ppm/°C, no DC-bias loss, no ageing; ranges to about 3 kV DC, −55 to +125 °C.

Film to 1 MHz

Film dominates DC-link until switching exceeds ~1 MHz; ceramic DC-link takes over above.

MLCC Capacitors



Stacked MLCC

Class I for SiC/GaN to +150 °C, 25 V–3 kV; stacked 3D packaging adds capacitance without PCB area.

OBC DC-link

200–1,500 µF at 300–500 V with ESR below 1.5 mΩ.

New Dielectrics: U2J

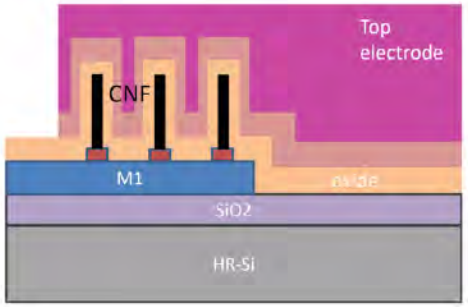
−750 ppm/°C linear TCC; more capacitance than C0G, low loss, for resonant tanks.

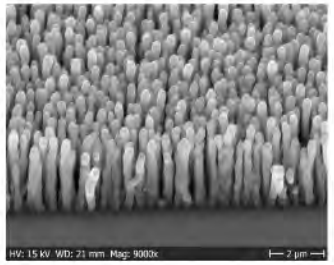
Material bottleneck

Sub-3 µm polypropylene film from very few plants; Torayfan +40 % vs ~20 %/yr EV growth.

Source: C0G HV MLCC for 800 V AI servers | EPCI Capacitors Technology Dossier 9/26

Silicon Capacitors: Subtractive vs Additive Technology



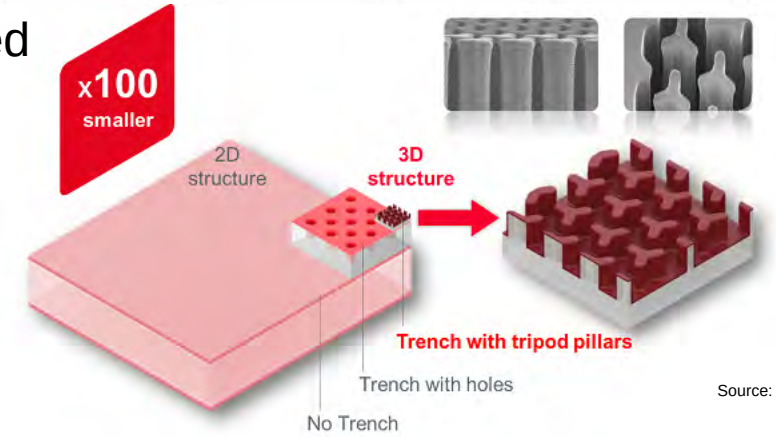


Conformal oxide deposition of HfO_2 and/or Al_2O_3 using ALD (< 250°C)

Source: Smoltek

Deep Trench Subtractive - Density From Geometry

SiO2 dielectric based



Source: Murata

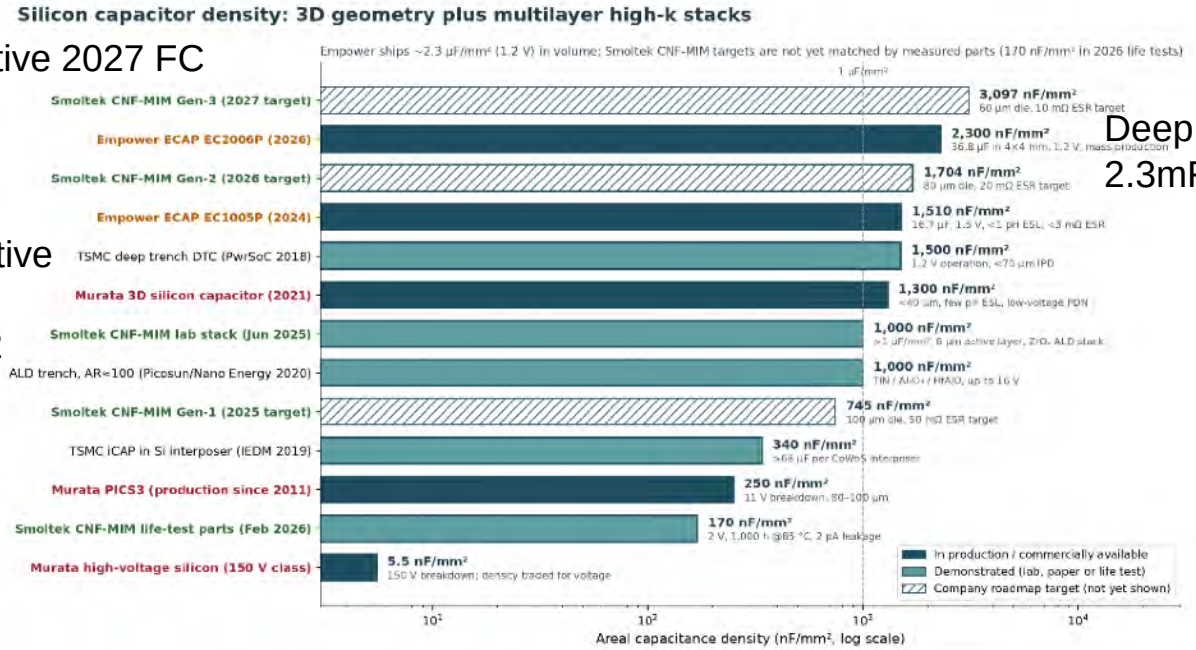
CNF-MIM High-k Stack ALD Additive Technology (IC wafer compatible process)

High *k* dielectric based

CNF Additive 2027 FC 3mF/mm2

CNF Additive 2025 Act 1mF/mm2

Deep Trench 2026 Act 2.3mF/mm2



USD 2.30 bn

silicon capacitor market 2026; growth estimates range 5–18 %

8 bn units

global deep-trench capacity in 2025, up 35 %

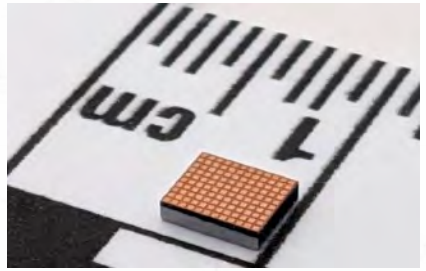
Silicon vs MLCC Capacitor Technology

CPU/GPU Coupling Integration

- Low parasitics, high frequency
- high ripple current

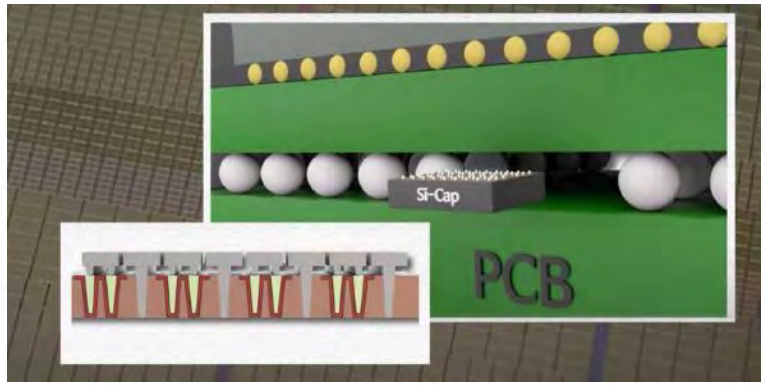
Under the GPU / Package Substrate / Embedding ⇦ ⇩ close proximity placement

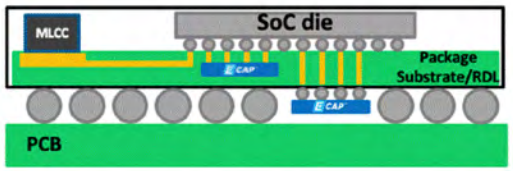
Empower releases 16.6 uF with sub 1 pH of ESL and 3 mΩ of ESR in a 120-pad configuration silicon capacitor for substrate core



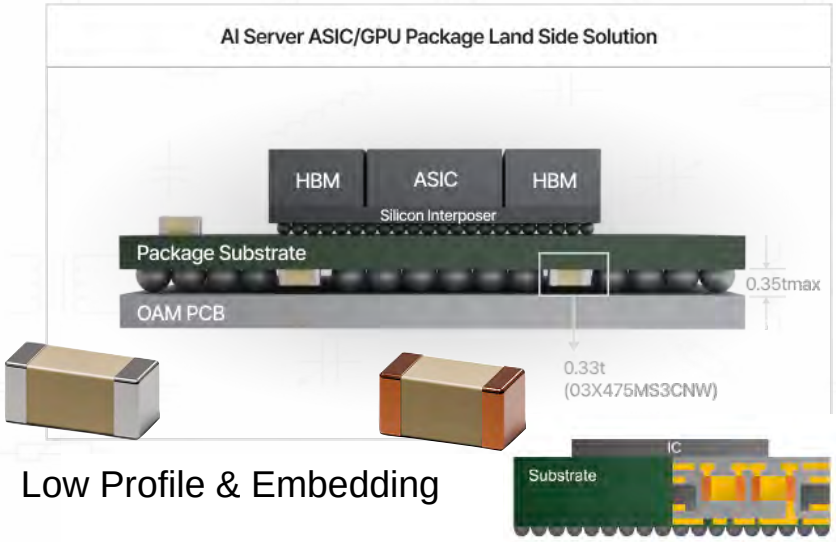
Silicon capacitors

capacitance density up to **2.5 uF/mm²**
stable capacitance performance
ultra-low ESL - single digit pH
ultra low ESR





MLCC capacitors



Low Profile & Embedding

Capacitance density calculation

MLCC Samsung Electro-Mechanics:
Ultra–High-Capacitance 4.7uF 2.5V MLCC in 0201, X6S for AI GPU

0201inch: 0.6x0.3mm = 4.7uF / 0.18mm² = **26uF/mm²**
strong dependence to DC BIAS, AC and temp

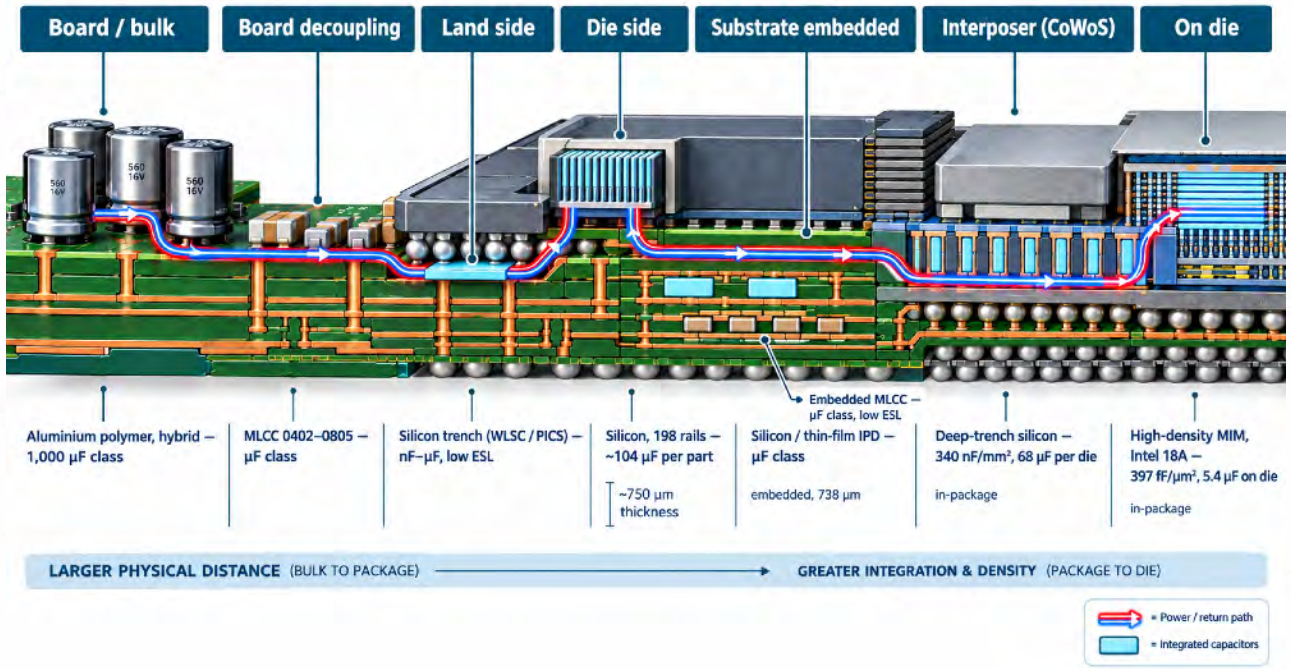
Effective Capacitance at 1.25V, small AC, 85C:
DC BIAS – 50% of rated = 13uF/mm²
AC small ripple – 40% = 7.8uF/mm²
temp 85C -7% = **7.2uF/mm²**

Source: Samsung CL03X475MS3CNW datasheet

https://passive-components.eu/empowers-low-esl-1ph-silicon-capacitor-meets-tight-ai-chip-requirement/

https://passive-components.eu/samsung-releases-ultra-high-capacitance-4-7uf-2-5v-mlcc-in-0201-for-ai-gpu/

Power Delivery Network Ladder



Over 200MHz Capacitance Moves Into Package

ESL and mounting inductance — not capacitance — set the PDN

High di/dt = low parasitic losses requirements = close proximity POL integration, embedding, IPDs, in package

PDN tier	Technology	Density / capacity	Thickness
Board / bulk	Al hybrid, Tantalum polymer	1,000 µF class per part	1.5–10 mm
Board decoupling	MLCC 0402–0805	µF class; ~0.50 nH mounting L per 0402	0.5–0.9 mm
Land side	Silicon trench (WLSC / PICS)	nF–µF; ESL ~15 pH typical	60–70 µm
Die side	Silicon, 198 rails	≈104 µF per part; very low ESL	750 µm
Substrate embedded	Silicon / thin-film IPD	µF class; typ. ESL ~10–30 pH at component level	738 µm
Substrate embedded	Embedded MLCC	µF class; typ. effective loop ESL ~50–200 pH	0.35-0.5 mm
Interposer (CoWoS)	Deep-trench silicon	340 nF/mm², 68 µF per die; low-pH ESL	In-package
On die	High-density MIM, Intel 18A	397 fF/µm², 5.4 µF on die; very low local loop inductance	In-package

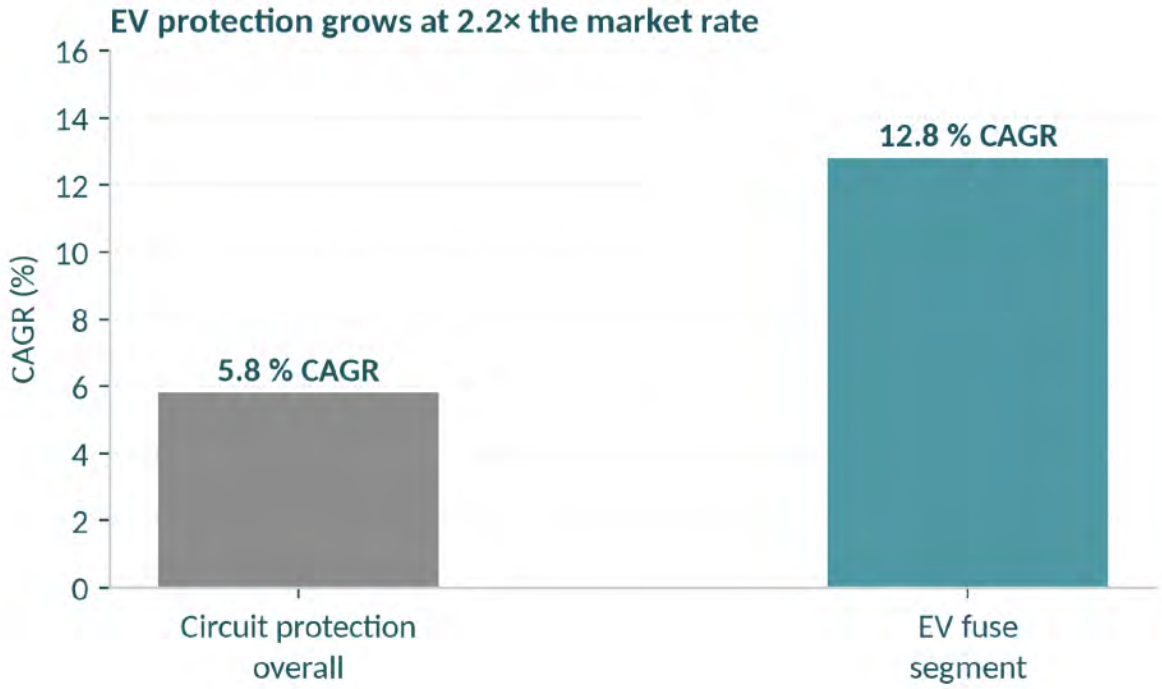
Single-digit mΩ impedance targets with sub-30 nH loop-inductance allowances per capacitor cannot be met by adding surface parts.

Everything above roughly 200 MHz is migrating into the package. On-die MIM at 397 fF/µm² combined with a 3.6 µF land-side capacitor eliminated a 50 A / 10 ns GPU droop of −300.4 mV. Deep-trench interposer devices show leakage below 1 fA/µm² at 1.35 V and 105 °C — these are production numbers, not research results.

Source: EPCI Technology Dossiers 2026 — passive-components.eu

Circuit Protection: Fastest-Growing Segment

Higher voltages and faster edges outrun the installed toolbox



Market EV fuse segment USD 2.5 bn at 12.8 % CAGR vs 5.8 % for protection overall.

Voltage 1,000 VDC fuses mandatory in 800 V architectures; automotive TVS families reach 540 V standoff and up to 5,000 W at 10/1000 µs.

Speed gap GaN/SiC edges need picosecond-class clamping the industry has not solved.

Standards IEC 61000-4-2:2025 Ed 3.0 adds the Ip2 parameter, CE deadline around early 2028.

Source: EPCI Circuit Protection Dossier | Littelfuse high-voltage TVS

Reliability Scrutiny Returns

Miniaturisation hits defect-density and degradation limits

PERCOLATION IN MOLDED INDUCTORS

A degradation mechanism in the default compact choice

Long-term high-voltage, high-temperature studies found percolation-type degradation in molded power inductors.

Rule: keep peak current at 60–80 % of specified Isat and verify the vendor’s Isat definition.

DEFECT DENSITY BEHIND DERATING

Thin dielectrics fail first

01005 defect rates run 2,000–4,000 ppm vs 500–1,200 ppm for 0201.

Parts failing 1,000 h at 125 °C and 2× rated voltage were thin-dielectric, high-layer designs (2.29 µm / 179 layers); 7.8–20.2 µm parts passed.

Source: EPCI Technology Dossiers 2026

Automotive

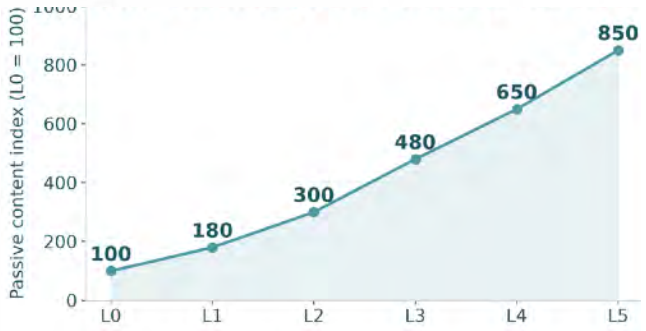
Power Electronics and Inverters present the fastest growing automotive electronics segment.

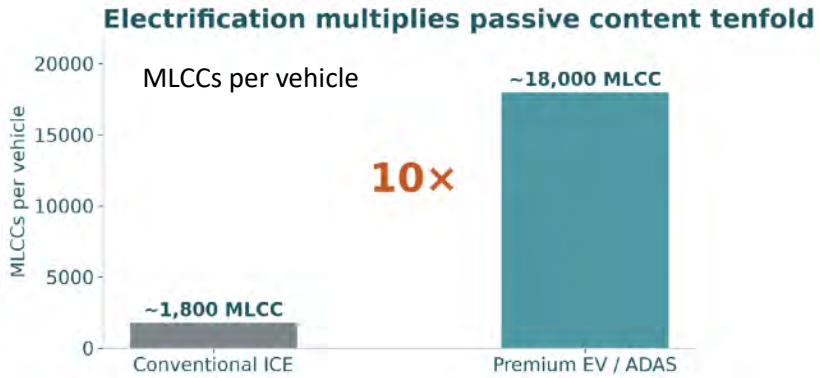
ADAS autonomy level drives passive content 8.5x.

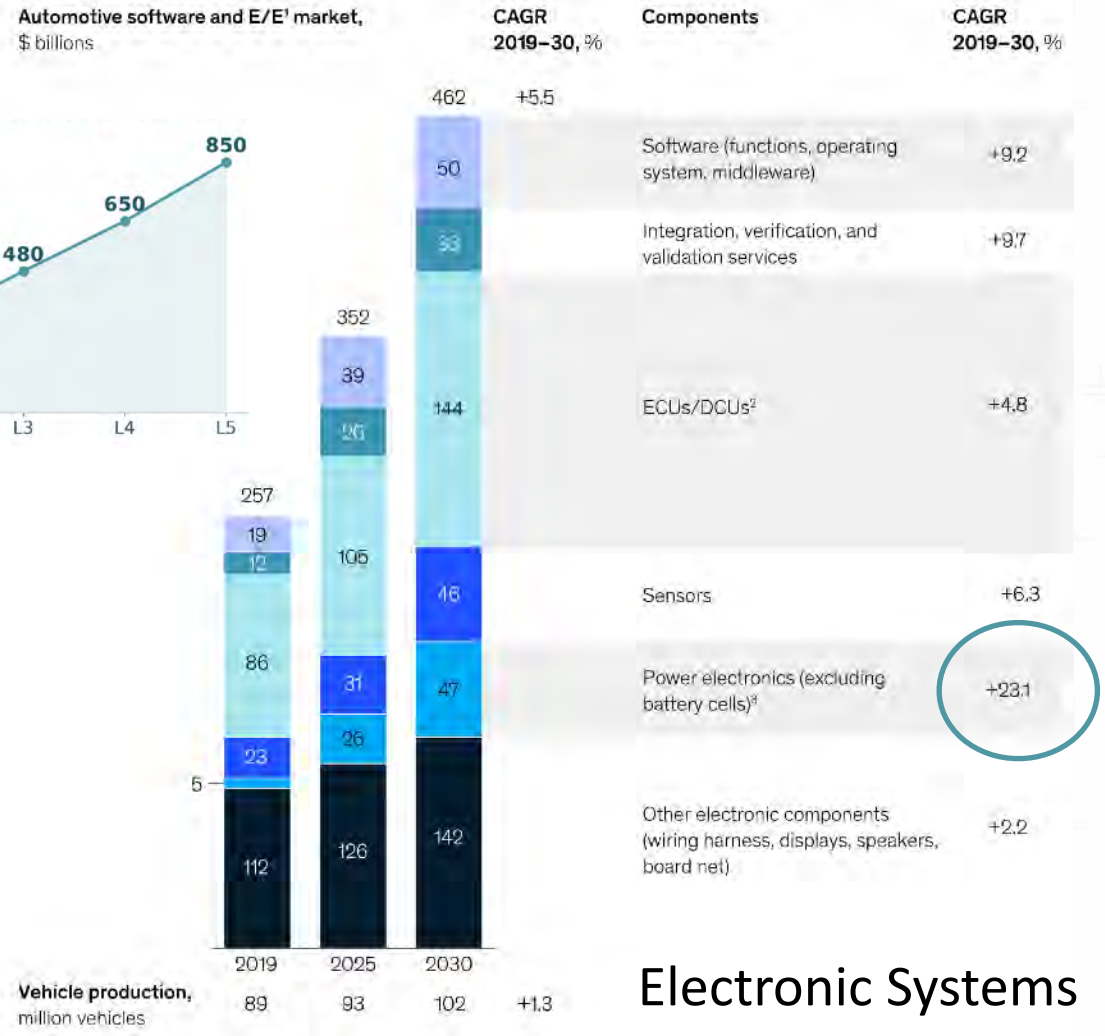
Per vehicle an EV carries 150–300 magnetic components, 1,500–2,800 resistors and 100–280 protection devices.

EMC filters count rises from 10 at L0 to 190 at L5 — noise suppression scales with autonomy, not with power.

Voltage 400 V → 800 V architectures demand 1,000–1,200 V-rated passives.







Electronic Systems

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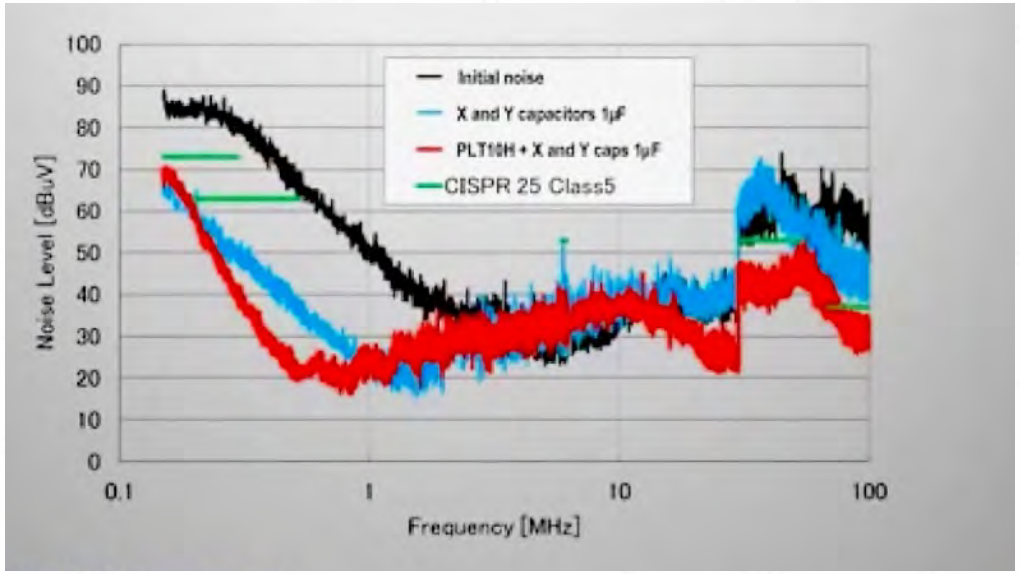
Automotive – EMC Challenges - Power Over Coax

High Power Switching & High Processing Power
& Lowering of Processor Voltage

NOISE SUPPRESSION & EMC SHIELDING CHALLENGES

High Speed Data Transmition

- **Integration & Miniaturization** of detection sensors (cameras, LIDAR, radar, etc…)
- **Power Over Coax** for image data transmission combines data and power transmission over a single coaxial line to reduce the amount of cable



Impact of safety capacitors and common mode choke to EMI suppression effectiveness

EMC Challenges - POC

CAN-FD high speed, high accuracy miniature ceramic resonators





Noise suppression by high current common (500mA) mode chokes in miniature 0201 case size

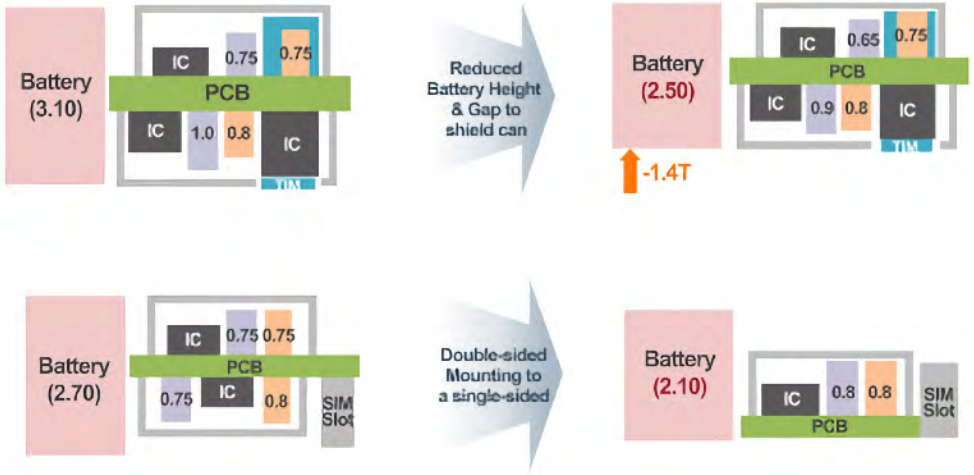
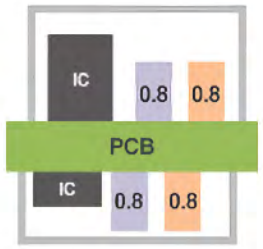
MLCC 10uF/25V in 2012 case size for 12V line smoothing applications in automobiles



source: Murata; passive-components.eu

Wearables

Reduce capacitor height, keep useful capacitance in tiny case sizes, and move decoupling closer to the load where possible.

Device	Foldable SMP		Smart Glasses	TWS
Year	'2024	'2025~	'2025	'2025
Set F/F				

SMP = Smartphones
TWS = True Wireless Stereo

Inductor MLCC



MLCC Capabilities

0.5 mm
Listed max thickness

4.7–22 µF
Capacitance

2.5–25 V
Rated voltage

source: Samsung

What Part 1 Means for Space Programmes

Space shares plants, powders and pastes with the AI upcycle

1. **Allocation follows contracts.** LTA holders get priority; low-volume hi-rel orders without agreements risk queueing behind AI demand.

2. **Lifecycle risk rises.** EOL notices and capacity reallocation threaten long-lifecycle QPL and EPPL parts — monitor at family and line level.

3. **Construction drift.** Metal thrifting and new electrode systems change parts under unchanged family names — demand change notification.

4. **Bridge grades multiply.** COTS-plus and HRA-type families fill the space between automotive and MIL/ESCC.

5. **Price is no longer the lever.** Qualification depth, traceability and early sourcing decide availability in 2027–2028.

LTA = Long Term Agreement
HRA = "High Reliability Alternative," a designation for component families designed, tested, and screened for higher-reliability applications.

Source: EPCI Capacitors Technology Dossier 9/26 | TrendForce high-end MLCC | Samsung MLCC outlook | KEMET HRA X7R

Part 1 in Five Sentences

The landscape before we turn to AI

1. The market is USD 28–51 bn depending on scope, growing ~6 % — while AI-relevant grades grow ~17 %.
2. The shortage is grade-specific and physical: layers, yields and line output, not money, set the pace.
3. 2026 broke price discipline: cumulative MLCC +15–40 %, tantalum ingot ×2.6, silver above 70 USD/oz.
4. Technology moves to effective values, mounted parasitics, 800 V ratings, silicon and integration.
5. Qualification depth and early sourcing — not price — decide availability for 2027–2028.

Source: EPCI Capacitors Technology Dossier 9/26 | EPCI Technology Dossiers 2026

BREAK

14:45 – 15:05

Part 2 starts at 15:05: AI cloud and physical AI — transforming passives for autonomous, flying, dual-use and space systems.

PART 2

15:10 – 16:00

AI Cloud and Physical AI: Transforming Passives

01 AI cloud HW requirements

02 Consequences to passive components technology

03 Physical AI: robots and edge

04 Flying and autonomous systems

05 Space: transfer and qualification

06 Dual use and Defense

07 Key Takeaways and Conclusion

AI Power Management - Performance vs Rack Power

AI Server Performance vs Power Consumption 2024 - 2026

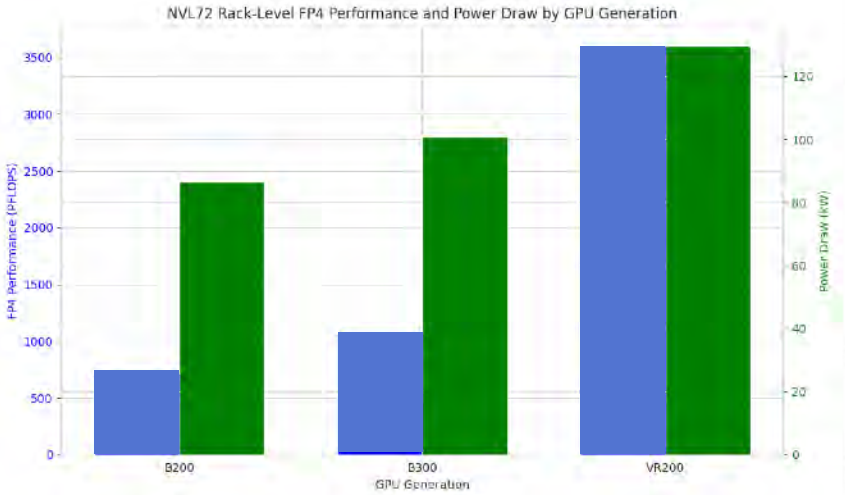
Model / Generation	Computing Power Increase	TDP / GPU	Cooling	Launch Window	Rack-Level FP4 (NVL72)	Rack-Level Power Draw
B200 (Blackwell)	Baseline (~10 PFLOPS)	1,200 W	Liquid (standard)	2024	~720 PFLOPS	~86.4 kW
B300 (Blackwell Ultra)	~+50 % (~15 PFLOPS)	1,400 W	Advanced liquid plates/manifolds	2025	~1,080 PFLOPS	~100.8 kW
VR200 (Vera Rubin, est.)	~+3.3× vs. B300 (~50 PFLOPS)	~1,800 W	Advanced liquid, immersion-ready	2026 (C2H)	~3,600 PFLOPS	~129.6 kW

5x 1.5x

Notes:

PFLOPS - PetaFLOPS = *peta* (10^{15}) floating-point operations per second.
A GPU rated at 15 PFLOPS **FP4** can perform 15 quadrillion FP4 operations every second under ideal conditions.

FP4 - Floating Point 4-bit, AI models often don't need full 32-bit or 16-bit precision to get accurate results. Using fewer bits speeds up computation, reduces memory use, and lowers power draw.



GPU Power to reach 1800W in 2026 (Vera Rubin)

Rack level Power Consumption to reach 130kW in 2026

CPU and Memory consumes ~80% of power energy

In two years from now

Performance increase 5x

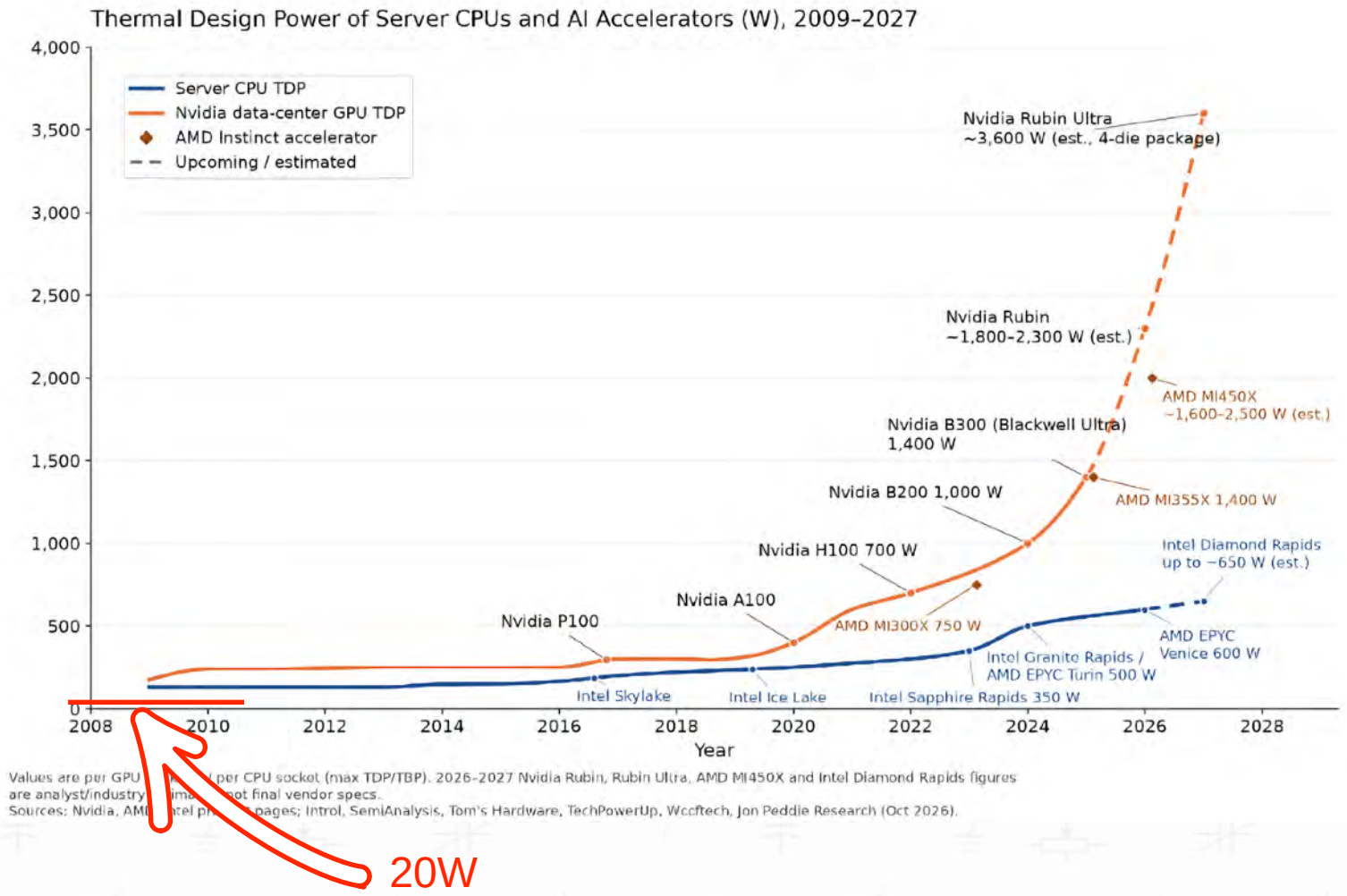
Consumption increase 1.5x

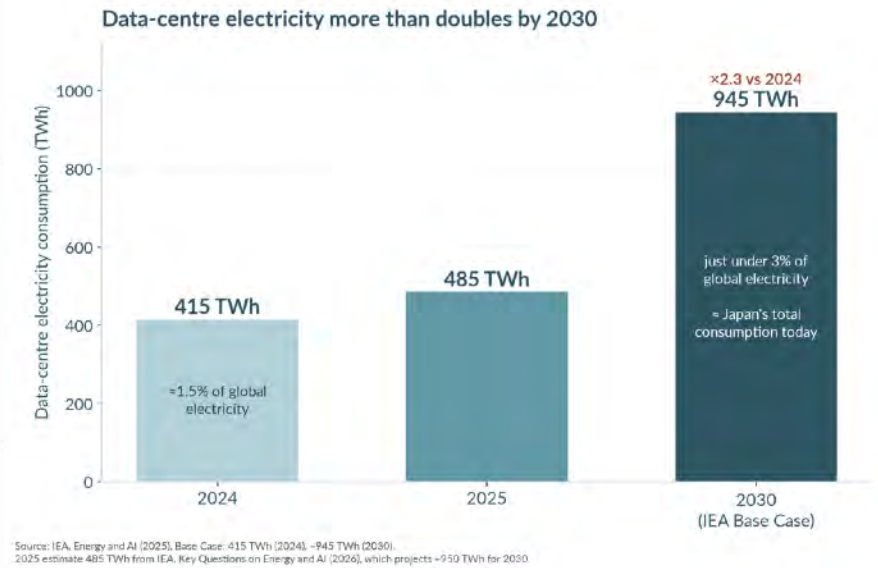


Power Delivery Challenges

- Voltage droop prevention during compute spikes
- Ultra-low ESR/ESL requirements for stability
- Severe space constraints near GPU/HBM
- High thermal density in compact packages

AI Power Demand





20W

How Many Watts Require Human Brain?

415 → 945 TWh

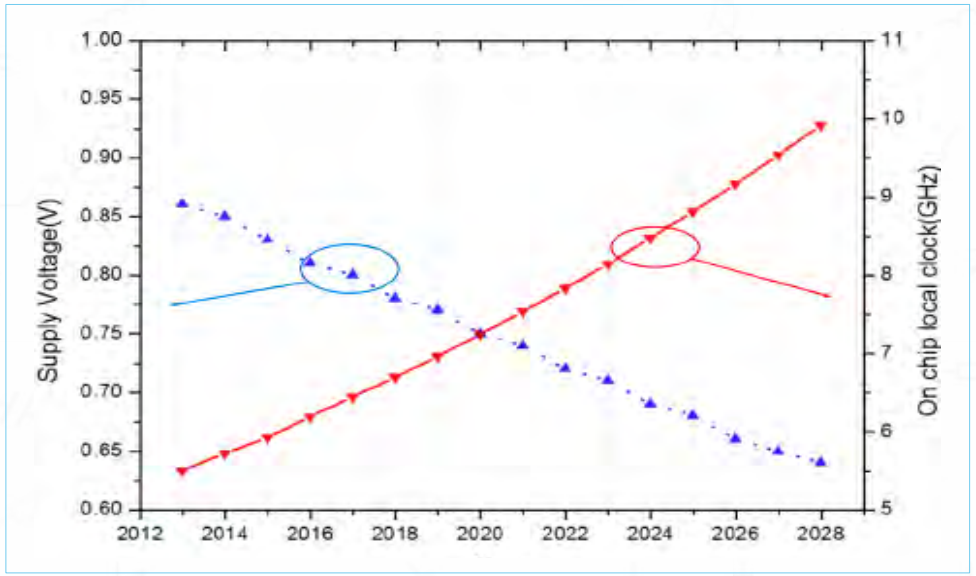
data-centre electricity 2024 → 2030 (IEA), just under 3 % of global demand

2–4 million

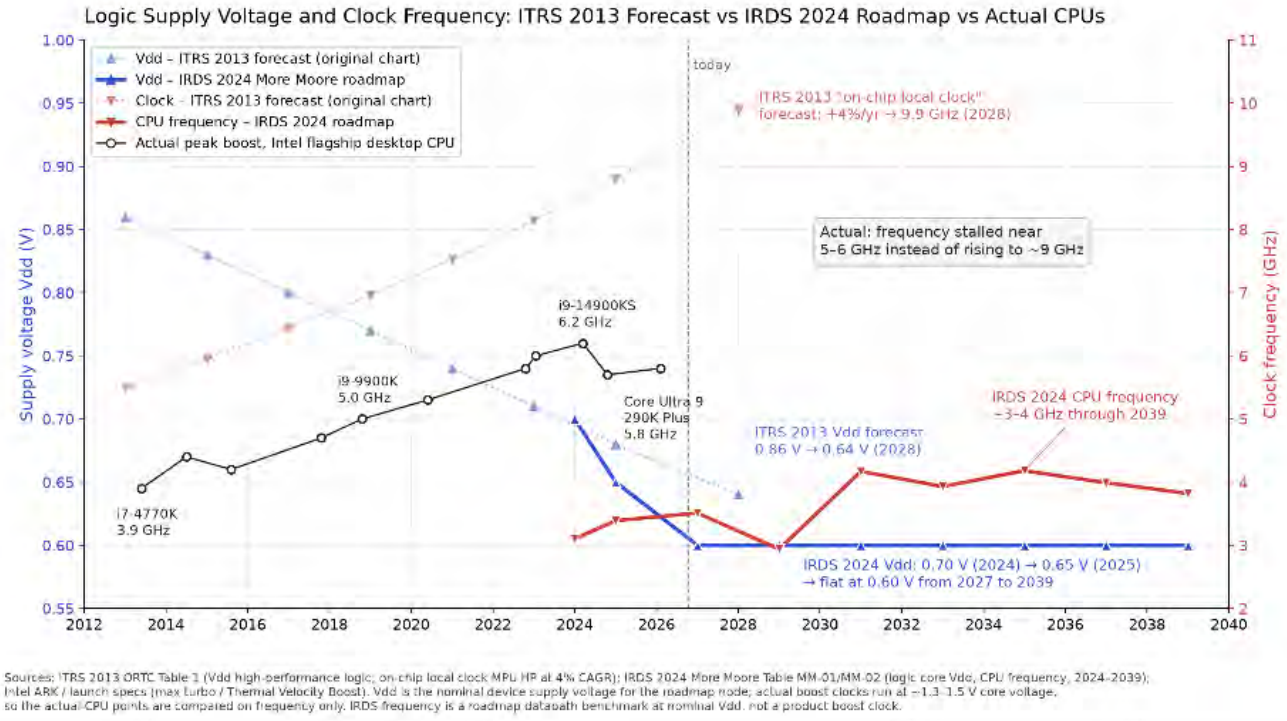
European households equal to a 1 % cut in data-centre conversion energy

CPU/GPU Development: Voltage - Clock Speed Trends

ITRS 2013 Forecast



2024 Roadmap and FC



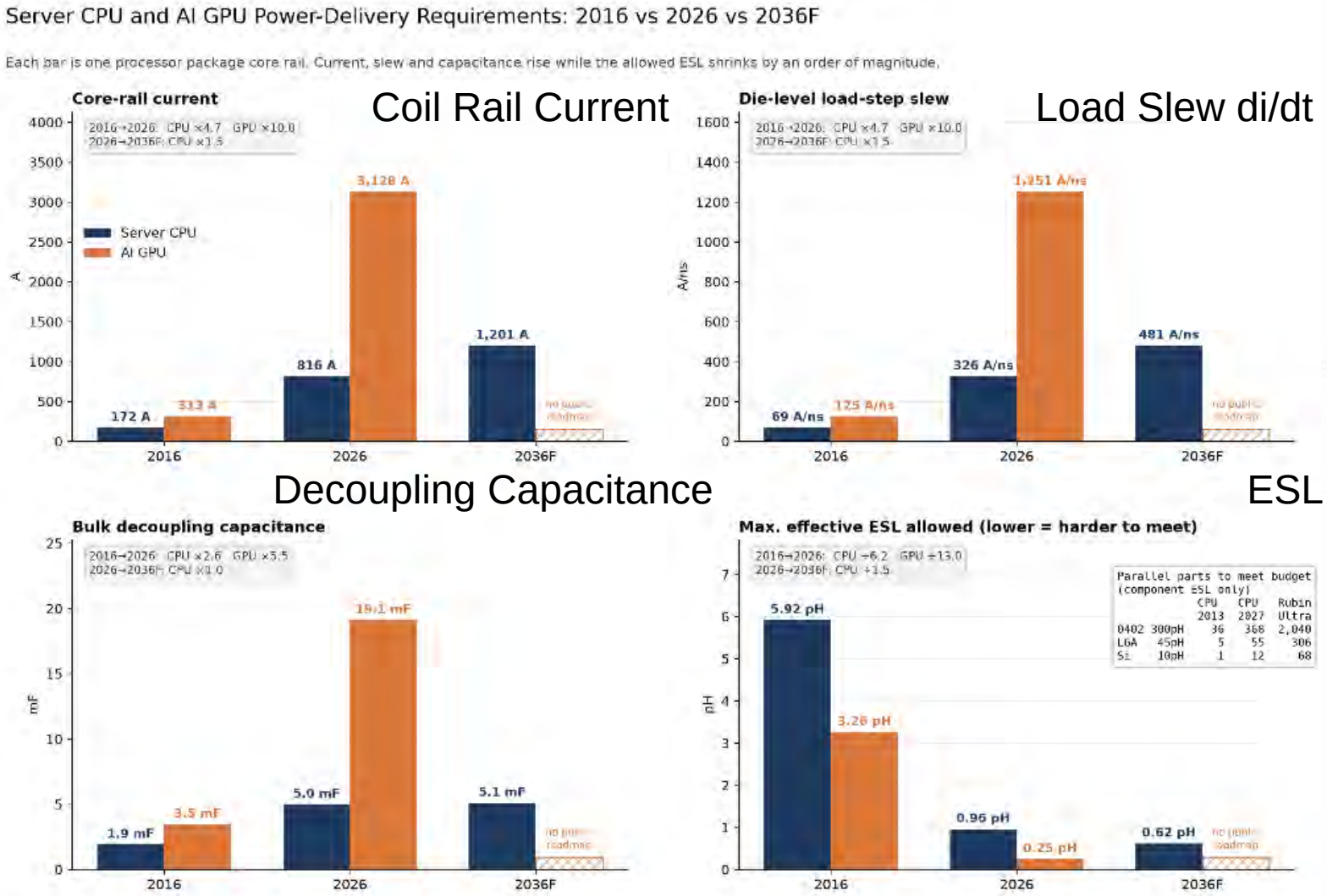
Sources: ITRS 2013 ORTC Table 1 (Vdd high-performance logic; on-chip local clock MPU HP at 4% CAGR); IRDS 2024 More Moore Table MM-01/MM-02 (logic core Vdd, CPU frequency, 2024–2039); Intel ARK / launch specs (max Turbo / Thermal Velocity Boost). Vdd is the nominal device supply voltage for the roadmap node; actual boost clocks run at ~1.3–1.5 V core voltage, so the actual-CPU points are compared on frequency only. IRDS frequency is a roadmap datapath benchmark at nominal Vdd, not a product boost clock.

CPU 2026 Trend: 3-6 GHz, 0.6V through 2039

Source: ITSC, KYOCERA AVX, Samsung

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CPU/GPU Development: Current, di/dt, Bulk Capacitance, ESL

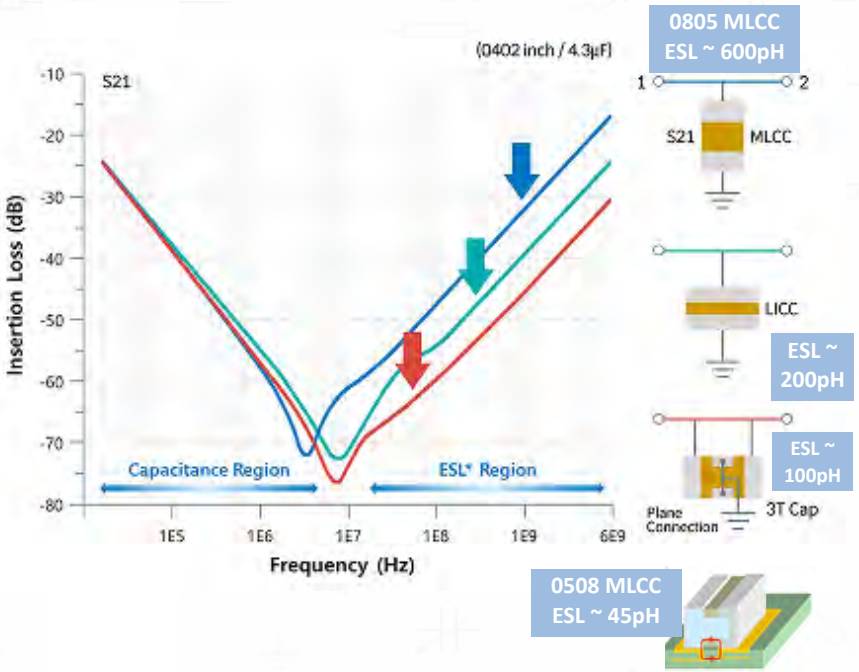


Coupling Capacitor Consequences

CPU/GPU processors require faster di/dt, making it essential to secure high capacitance decoupling while maintaining low ESL in smaller package sizes.

"AI MLCC's Law"
The MLCC capacitance required per GPU doubles every year.

Samsung Electro-Mechanics, Sep 2026



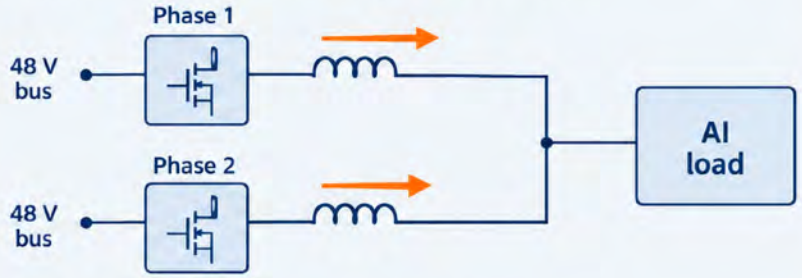
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How to Achieve di/dt Needs - TLVR

TLVR: a magnetic transient accelerator for AI processor power

Coupled inductors help the VRM respond to ultra-fast AI load steps.

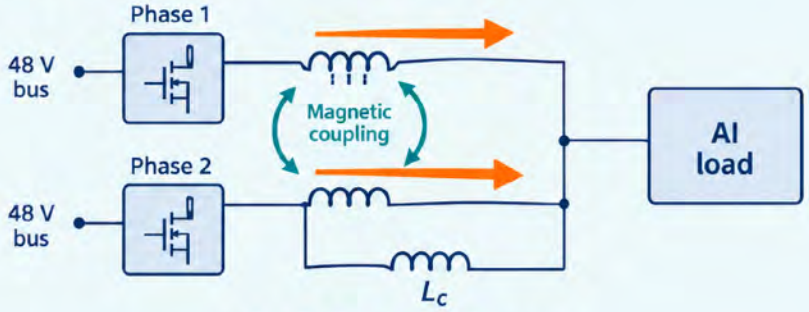
Conventional multiphase buck



267 A/µs

Voltage-limited current ramp → deeper voltage droop

TLVR coupled-inductor VRM



1,000 A/µs

Magnetic transient assist → faster current recovery

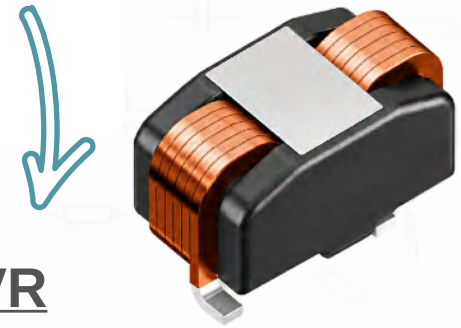
~3.7× FASTER CURRENT SLEW RATE

Transient magnetic coupling accelerates di/dt — not extra energy.



SiC/GaN improve upstream conversion; TLVR solves the final low-voltage transient bottleneck.

AI PM di/dt Load Challenge



TLVR

Coupled Inductors

Interleaving four phases at 300 kHz give an output ripple frequency of ~1.2 MHz.

Trade-off low ballast inductance speeds transients but raises ripple — the ballast value must be optimised against load current.

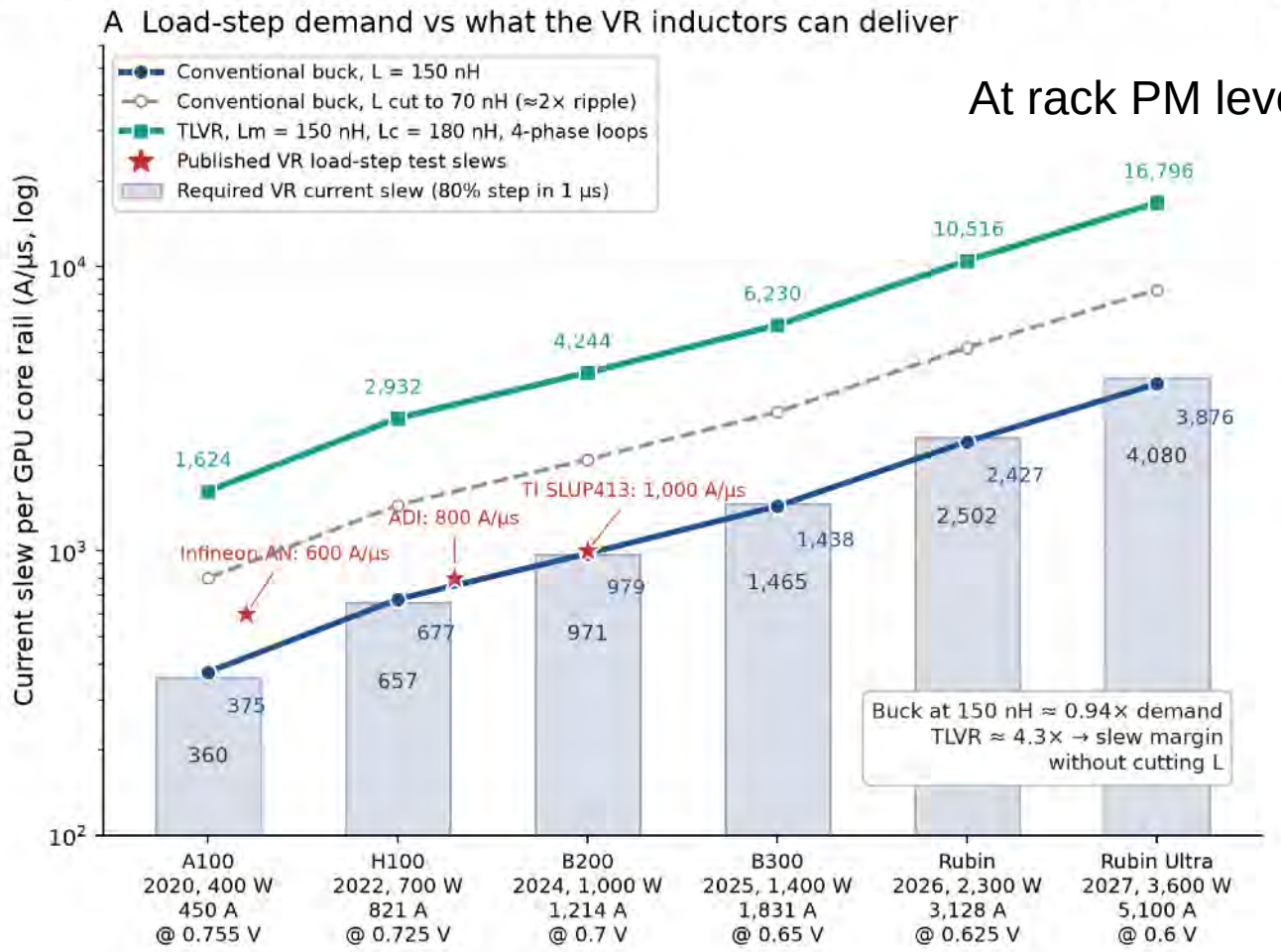
See more: https://passive-components.eu/tlvr-coupled-inductors-enabling-fast-load-step-response-in-multiphase-vrms/

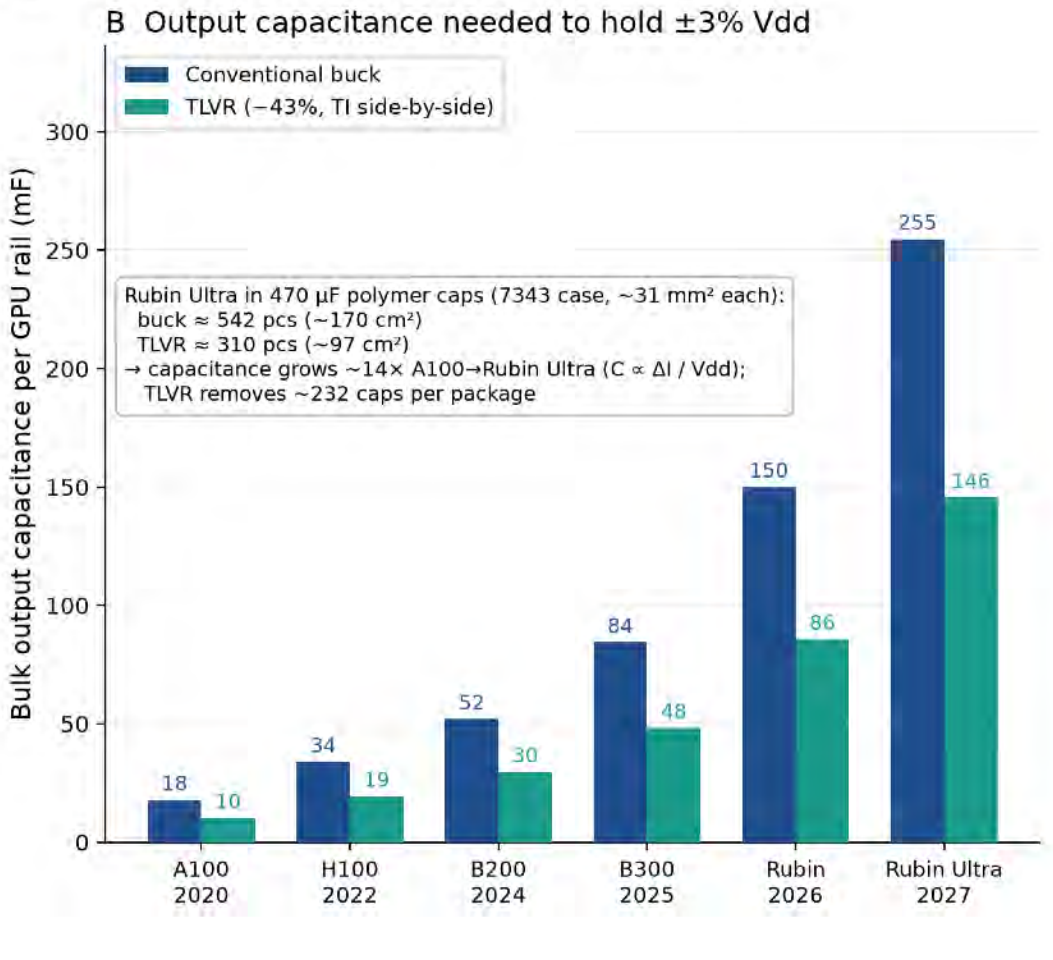
A **TLVR (Trans-Inductor Voltage Regulator)** replaces separate phase inductors with a coupled-inductor structure. When the load steps, the magnetic interaction between phases develops an additional transient voltage that assists current transfer/ramp-up in the phases that need it.

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How to Achieve di/dt Needs - TLVR

TLVR - 4x Current Slew Rate Increase and 43% Reduction of Output Capacitance

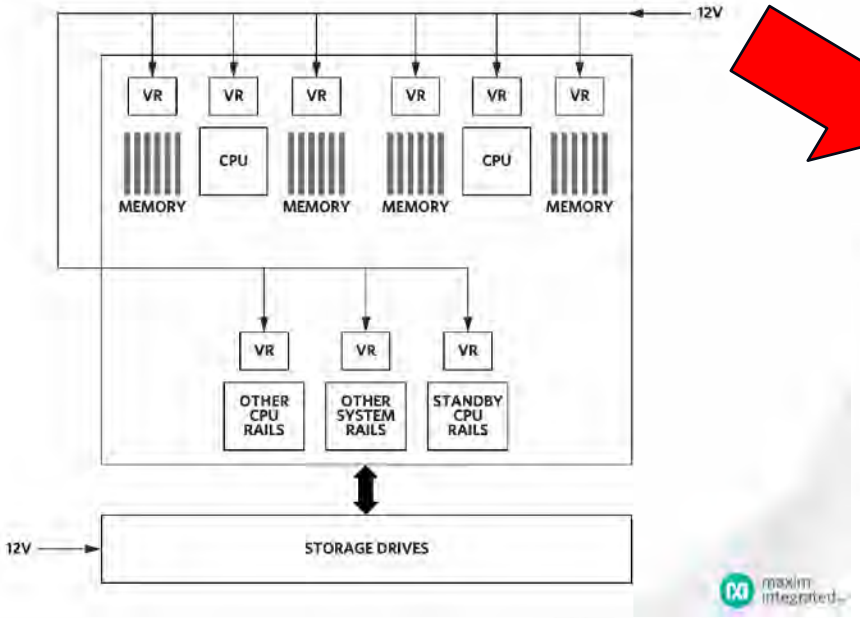




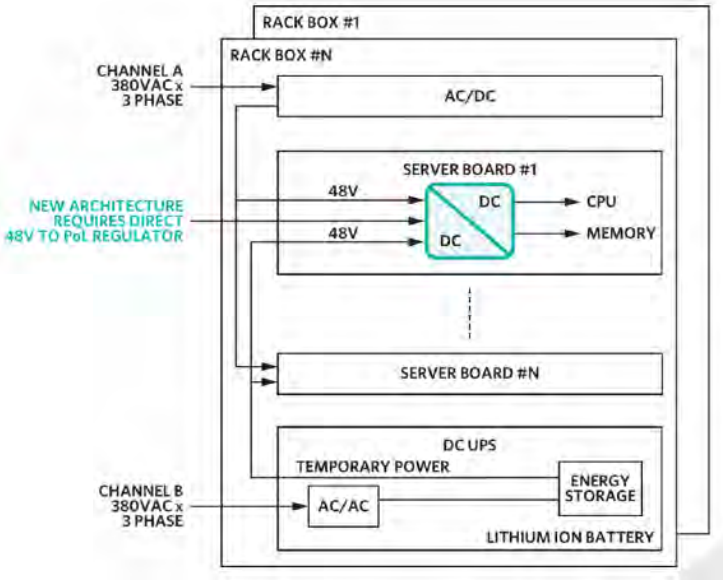
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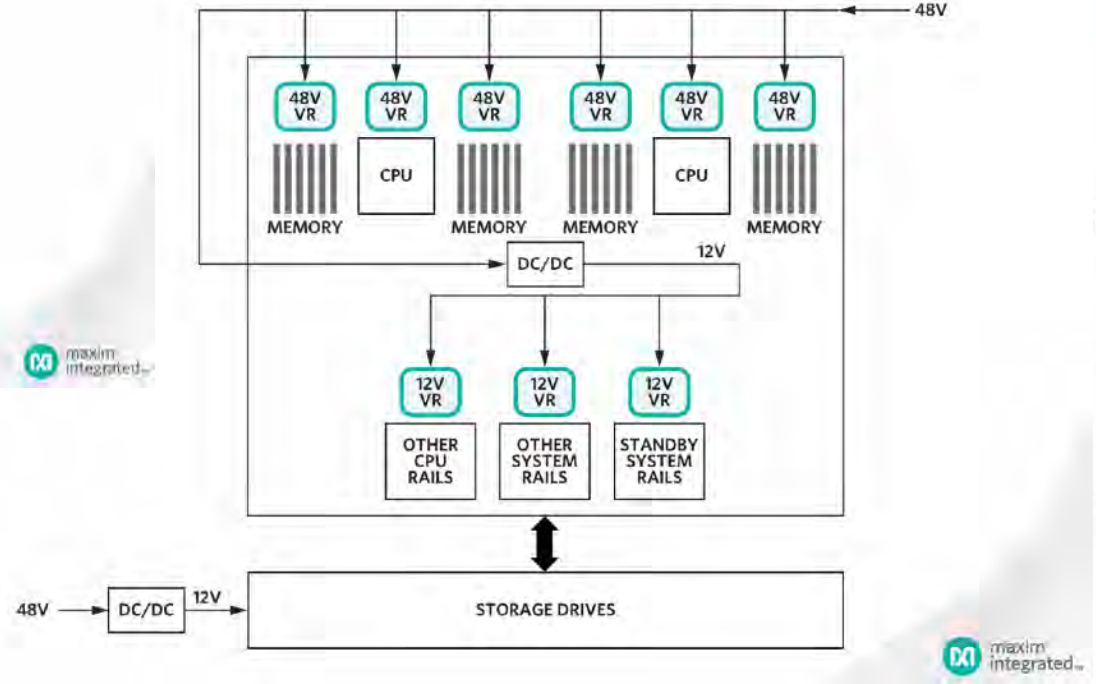
AI Power Management - Rack Power

12V Server Motherboard Power Architecture



48V/54V Server Motherboard Power Architecture





48V Power Rack Energy Savings

- > Up to 30% less conversion losses
- > 16x less power distribution losses

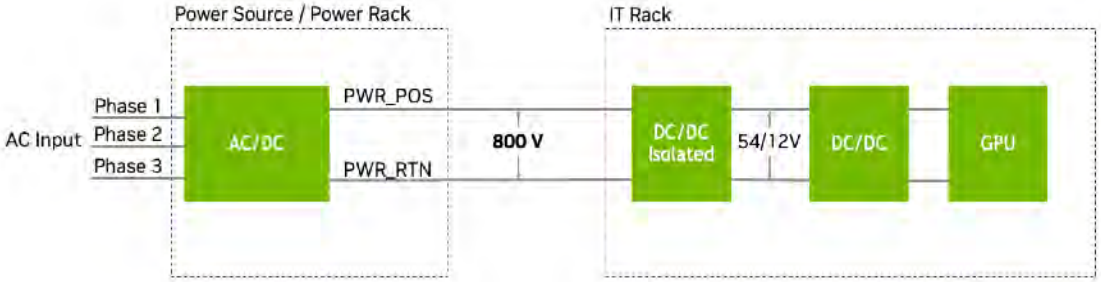
Open Rack V3 Power Shelf voltage is 51 V nominal, with a range of 46 V to 52 V, or 54 V nominal, with a range of 52 V to 56 V. The power is connected through four connectors, each rated at 100 A, for a total power of about 20 kW. The current trend is increasing from 20 kW shelf to 30 kW or more

Source: Maxim Integrated: New 48V Rack Power Architecture For Hyperscale Data Centers

AI Power Management - Rack Power

800 VDC Architecture - NVIDIA 2027 Requirements

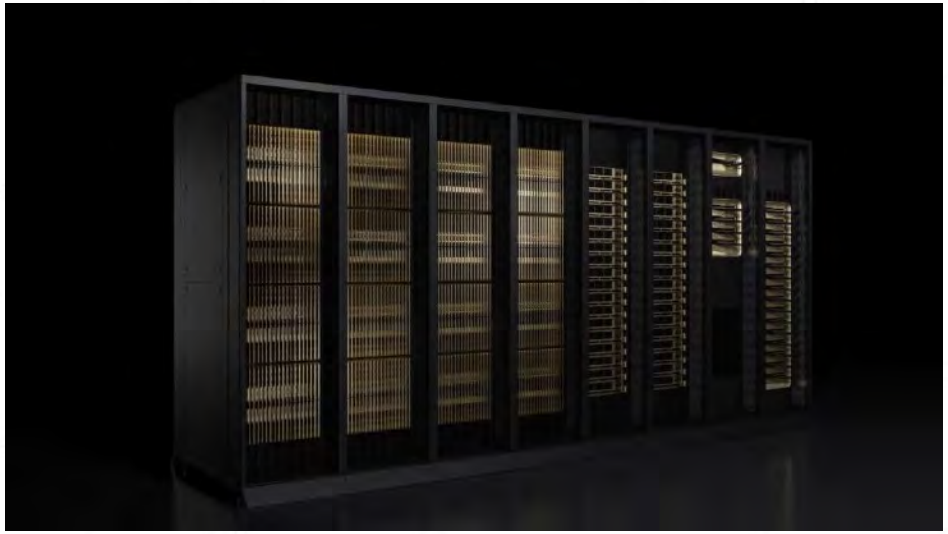
"Traditional 48/54 V in-rack power distribution, designed for kilowatt (KW)-scale racks, isn't designed to support the megawatt (MW)-scale racks coming soon to modern AI factories. "



NVIDIA is leading transition to 800 VDC data center power infrastructure to support 1 MW IT racks and beyond, starting in ***2027.*** *To accelerate adoption, NVIDIA is collaborating with key industry partners across the data center electrical ecosystem.*



NVIDIA 800 VDC architecture minimizes energy conversions



Key efficiency gains

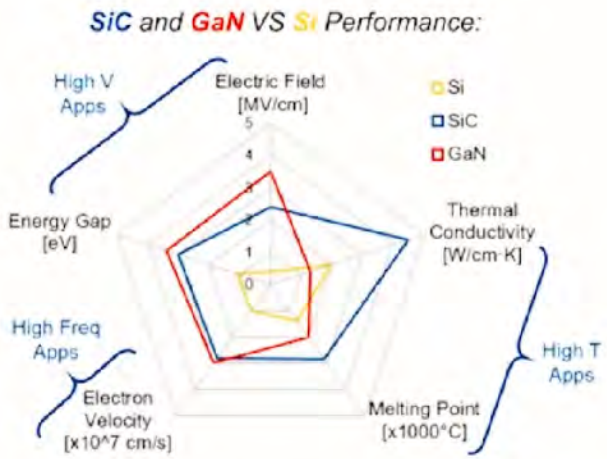
- Up to 5% improvement in end-to-end power efficiency
- Maintenance costs reduced by up to 70% due to fewer PSU failures and lower labor costs for component upkeep
- Lower cooling expenses from eliminating AC/DC PSUs inside IT racks
- Cost reductions in copper usage and thermal losses across the data center backbone.

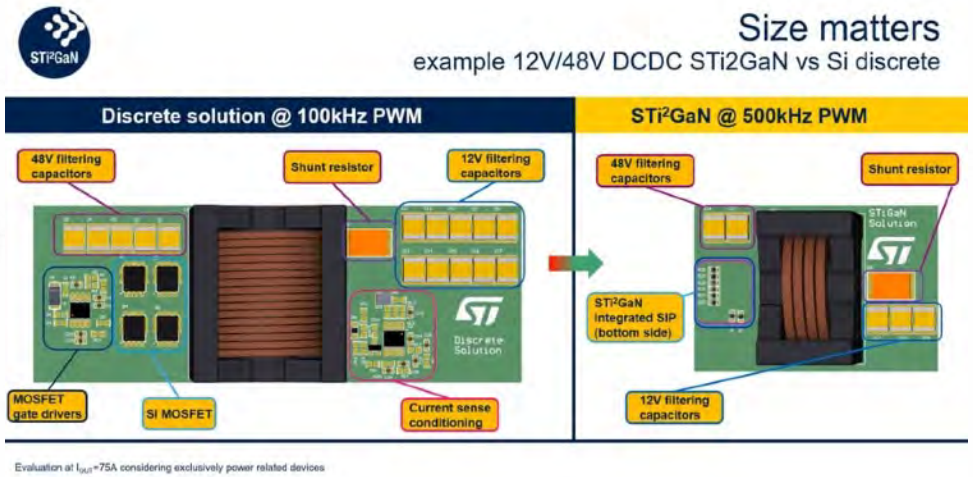
Source: NVIDIA PR: May20, 2025 https://developer.nvidia.com/blog/nvidia-800-v-hvdc-architecture-will-power-the-next-generation-of-ai-factories/

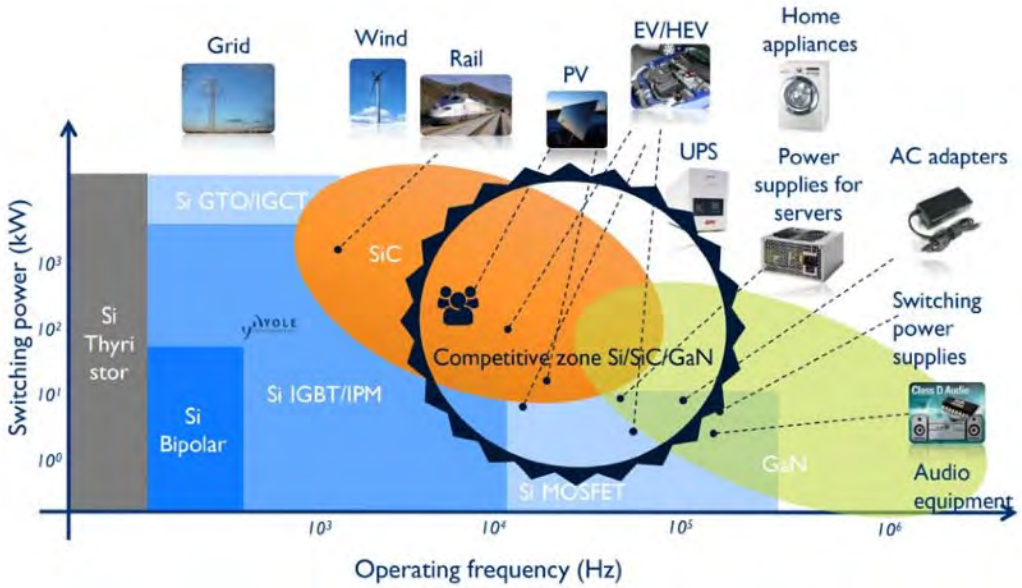
AI Power Management - Wide Gap Semiconductors Rack Power

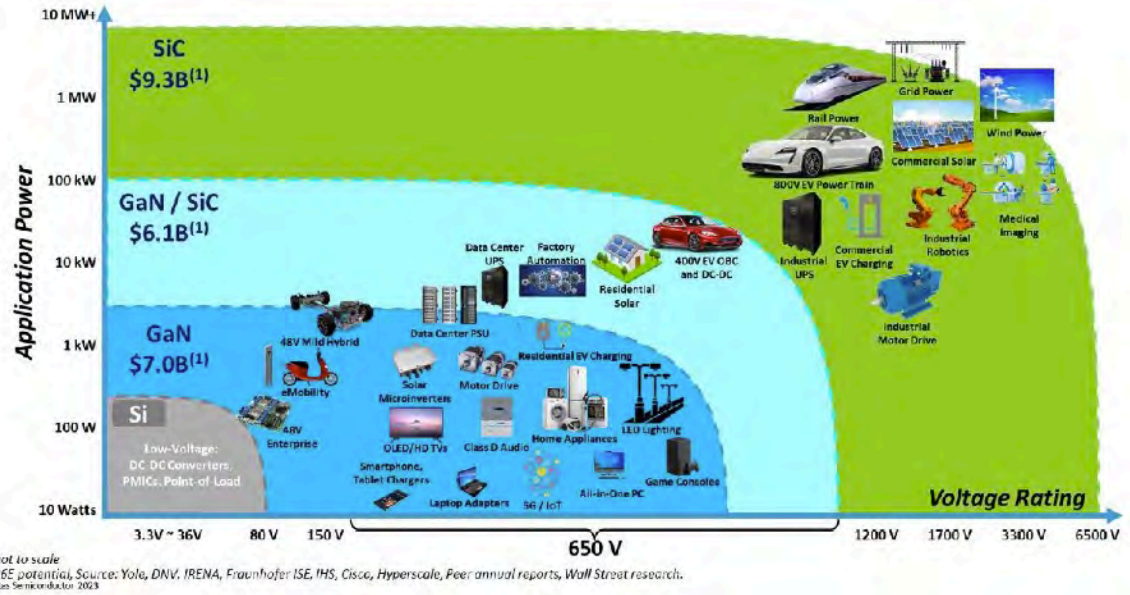
Semiconductor IC Development – Wide Gap GaN/SiC

- **High V / T / f benefits**
- Manufacturing and Cost Challenges









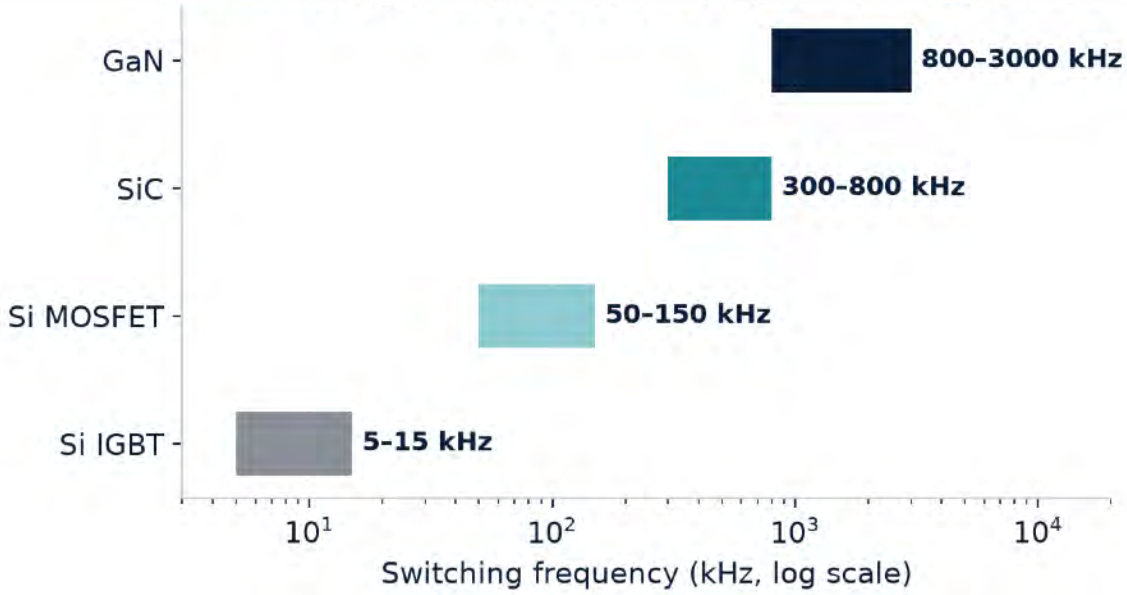
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AI Power Management - Wide Gap Semiconductors Rack Power

Wide-Bandgap Relocates the Challenges Into Magnetics and Passives

50–150 kHz → 300–800 kHz and beyond: 30–60 % magnetic volume reduction, but new material and thermal limits

"Magnetics set the achievable efficiency, power density and manufacturability before the semiconductors do."





Cores nanocrystalline and metal-composite become mandatory above ~300 kHz; >60 % loss reduction at 1 MHz.

Film capacitors pushed to 105–125 °C; low-ESL modules down to 8 nH; ultra-low-inductance traction parts launched 2026.

Ceramics C0G/U2J displacing X7R in high-ripple duty; DC-link capacitance falls from mF to hundreds of µF at SiC ≥ 25 kHz.

Protection SiC dv/dt is roughly 3× Si IGBT; GaN/SiC demand picosecond clamping the protection industry admits it has not yet solved.

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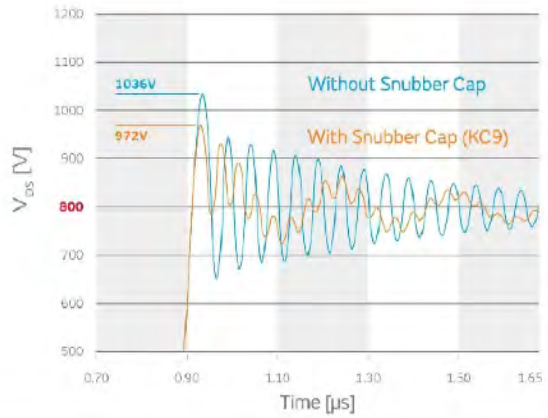
AI Power Management - Wide Gap Semiconductors Rack Power

PDN Based on Wide Gap Semiconductors

Switching Dynamic Load Challenges

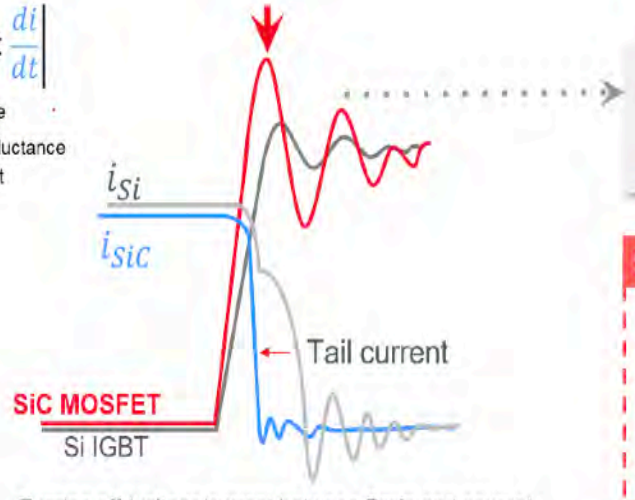
Transients, Oscillations, EMC, Safety …

Make Snubber capacitor, Safety capacitors, Circuit protection devices more critical



$$v = \left| -L \times \frac{di}{dt} \right|$$

v : Peak voltage
L : Parasitic inductance
i : Drain current
t : time



Turning off (voltage/current between Drain and source)

Snubber capacitor is more necessary



Voltage 1,000 VDC-rated fuses are now mandatory in 800 V architectures.

EV fuse market USD 2.5 bn, 12.8 % CAGR versus 5.8 % for circuit protection overall.

Speed gap GaN/SiC edges demand picosecond-class clamping

New standards IEC 61000-4-2:2025 Ed 3.0 introduces the Ip2 parameter, with a CE deadline around early 2028.

Safety Capacitors



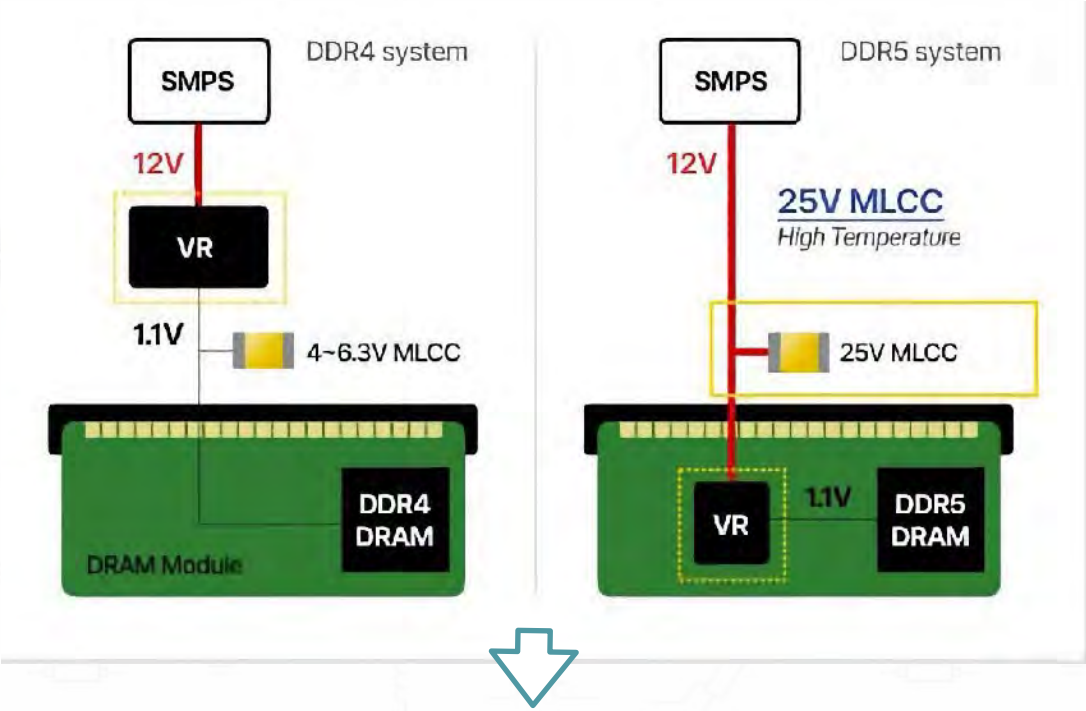
increase creepage distances for high-voltage applications

Source: Murata

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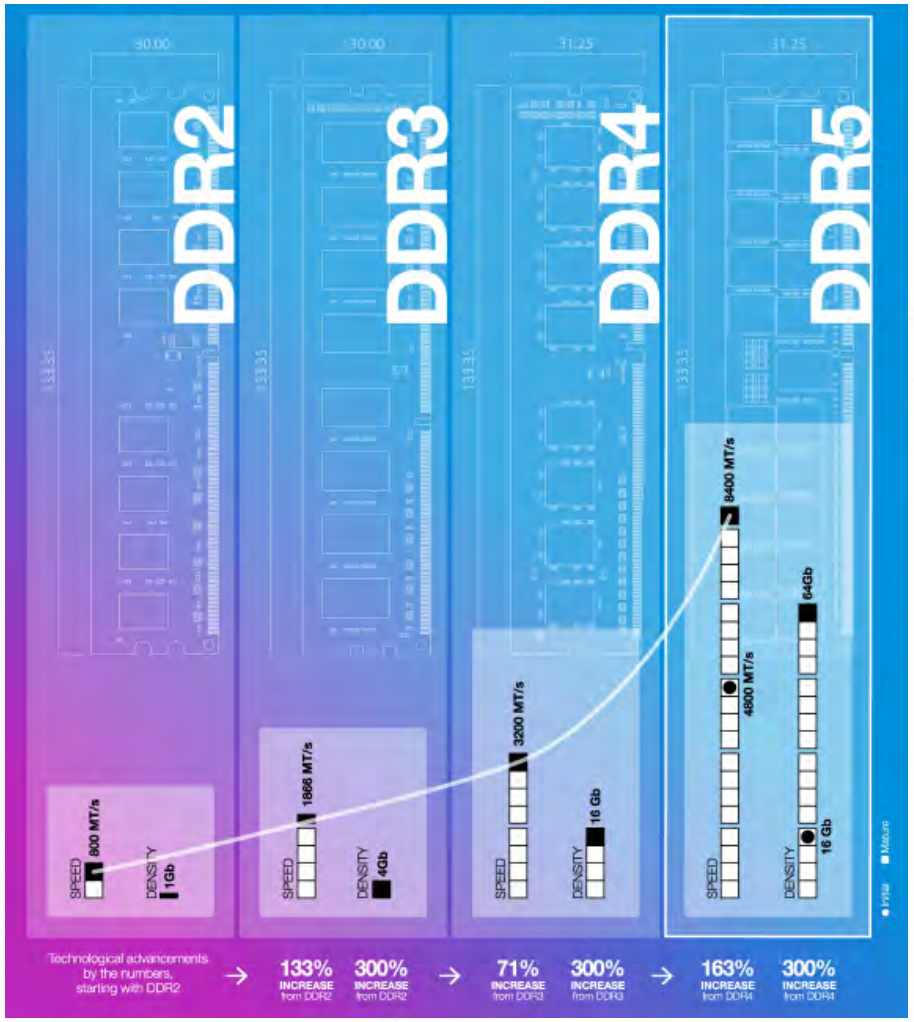
DDR4 to DDR5 Memory

- DDR5 Memory architecture offers up to **50% higher data rates**
- **10-20% better energy efficiency**
- **Greater capacity per DIMM** – Higher-density modules mean you can feed large models without spilling to slower storage
- **Improved parallelism** – More independent banks allow multiple AI threads to access memory simultaneously without as many stalls
- **Challenge:** Complete architecture and memory power architecture re-design



Passive Components DDR5 PM selection change from 4/6.3V (Ta/MLCC) to 25V MLCC (MLCC sole solution)

DDR Memory Evolution



Source: Micron

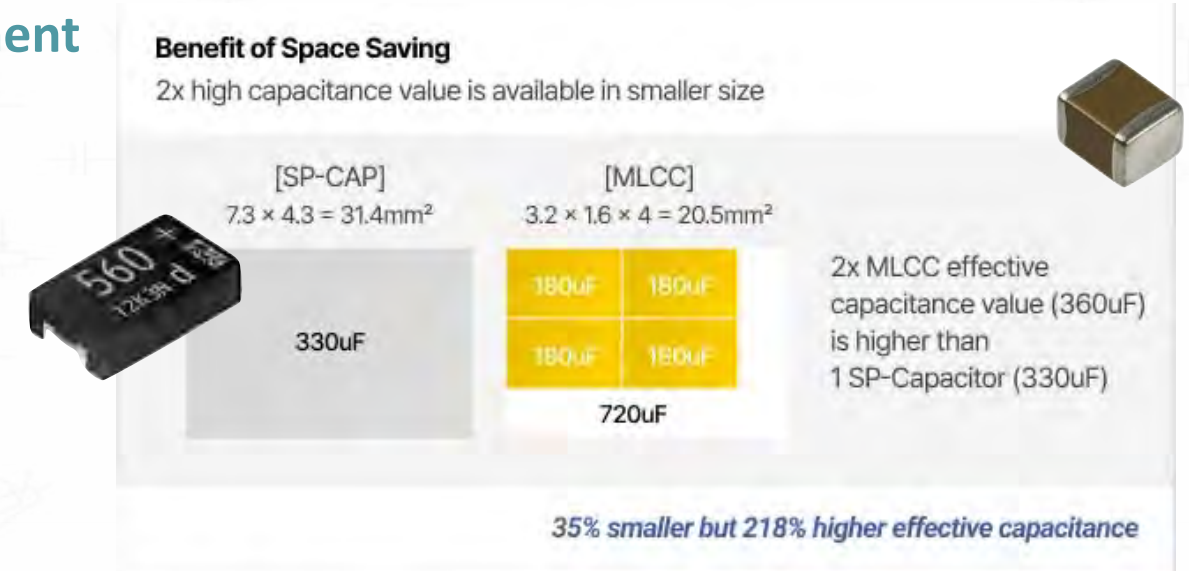
MLCC Development

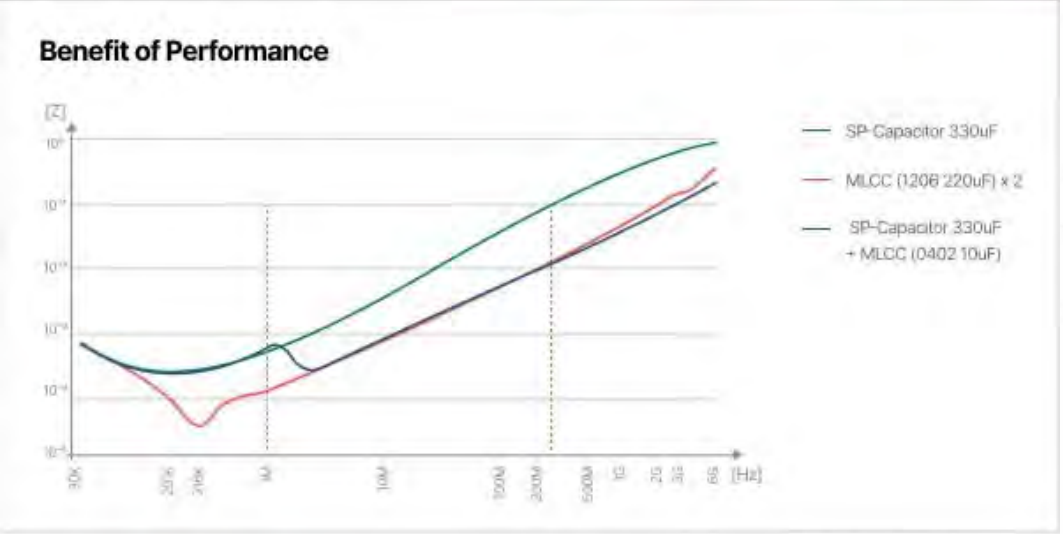
MLCC Aiming Bulk Electrolytic Capacitor Replacement

GPU/CPU Power Management Bulk Capacitors Replacement

- MLCC try to offer alternative to Al polymer chips
- Low voltage 2.5/4V capacitors
- Downsizing at “effective capacitance” with lower impedance performance

	10uF	22uF	47uF	100uF	220uF	330uF
0402	4V X6S	4V X6S		General Server		AI Server
0603		4V X6S	4V X6S			
0805			4V X6S	4V X6S		
1206				4V X6S	4V X6S	
1210						2.5V X6S





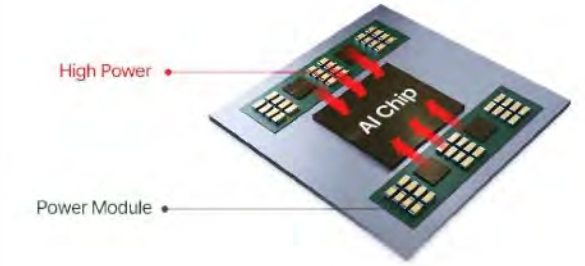
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MLCC Development

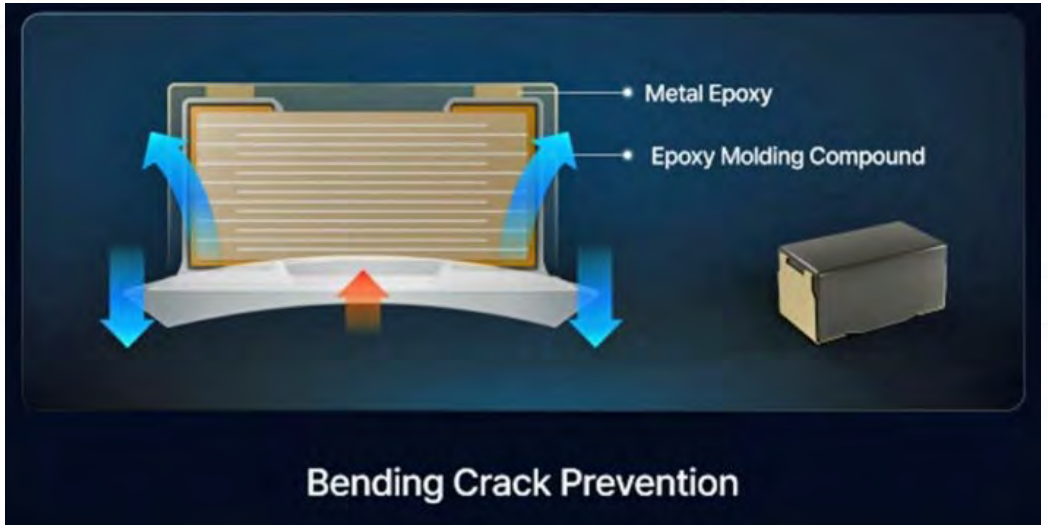
MLCC Capacitors for 48-52V Rack Power Voltage

- Samsung Releases 4.7 µF 100V in 1206 inch 3216 metric X7S dielectric
- Murata and TDK Releases 1 µF 100V in 0603 inch 1608 metric X7R
- Murata Releases 10µF/100V X7S MLCC in 1210 inch size 3225 metric

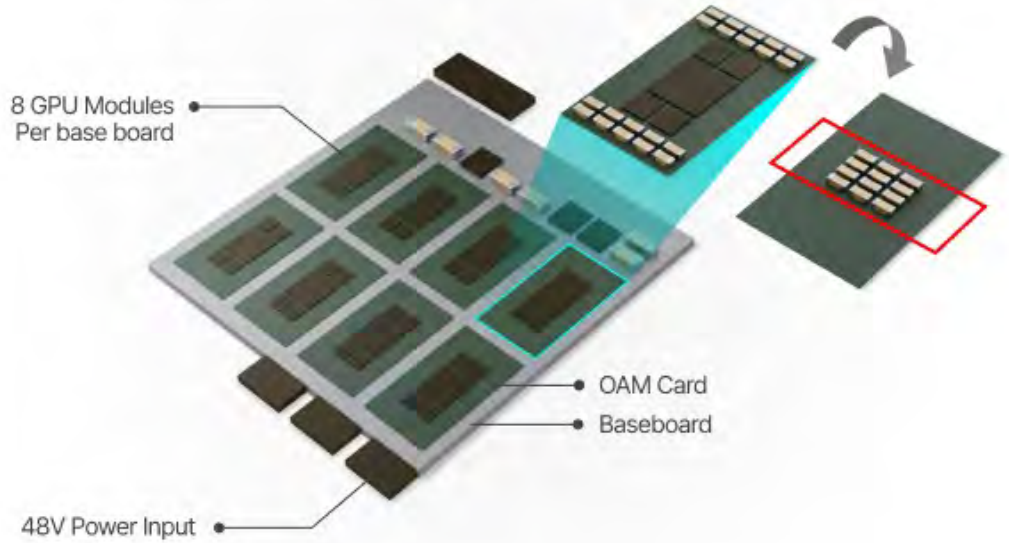




molded frame MLCCs to suppress flex issues in 1210 size (4.7uF 100V) specifically targeting AI server boards



https://passive-components.eu/samsung-electro-mechanics-releases-molded-mlcc-capacitors/

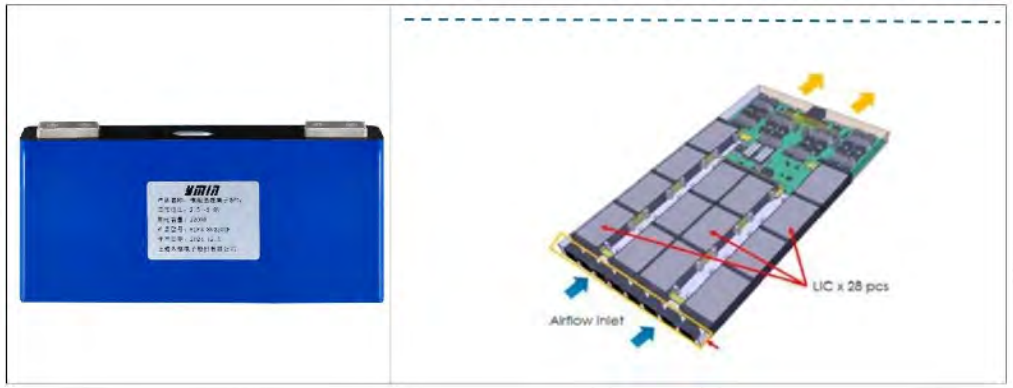


source: Samsung Electro-Mechanics, Murata, TDK

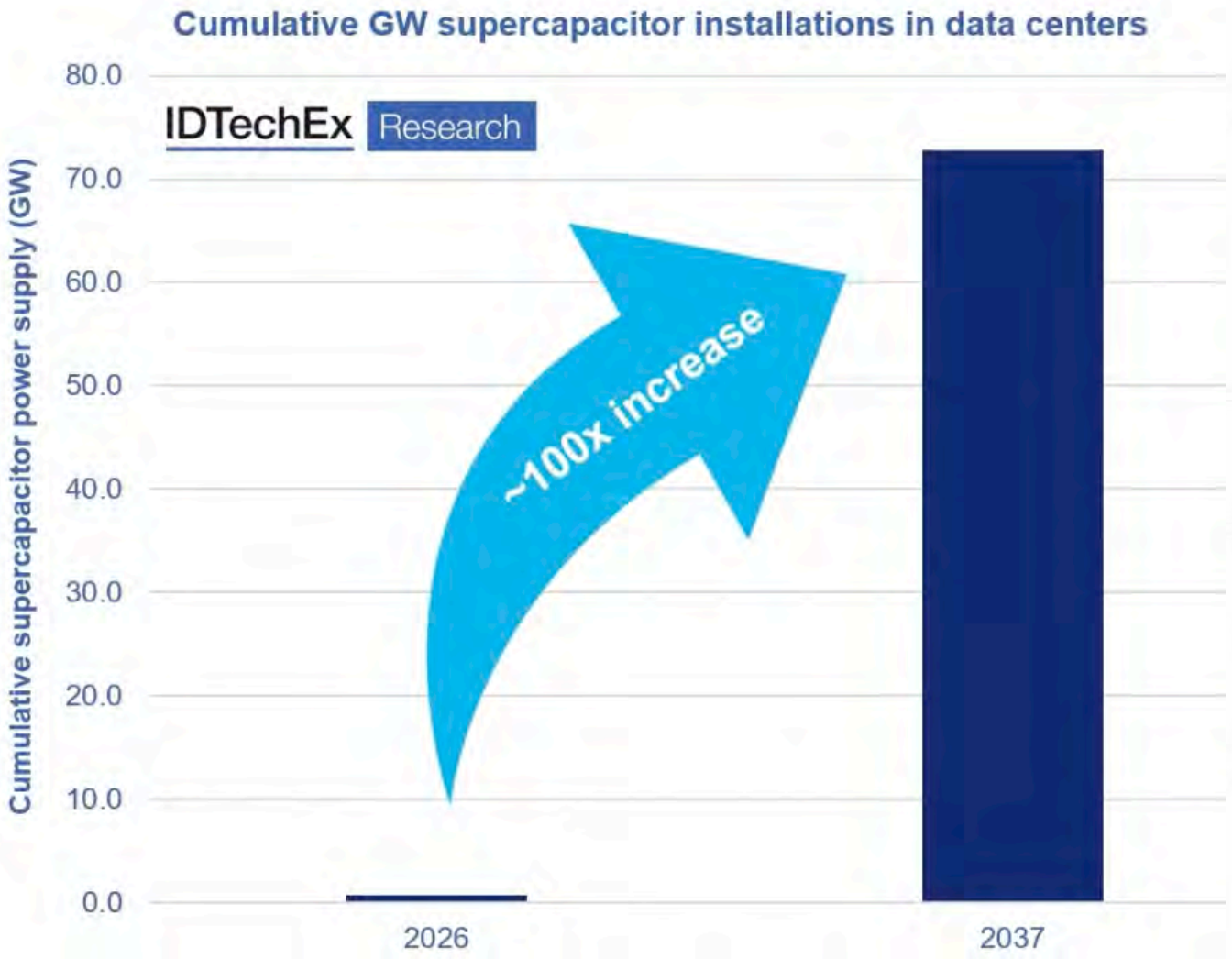
Supercapacitor Based Energy Storage System

AI Induces Fast Transient Dynamics Challenges to Power Grids: Sudd consumption can strain the grid, leading to instability or the need for infrastructure.

NVIDIA unveiled GB300 server, with integration of supercapacitors int power system



Ymin supercapacitors shows use of 28 pcs of their LiC supercapacitors
Yongming Electronics developed PPS (Power Pulse Supercapacitor) module
SLF 4.0 V 4500 F square SC, ESR < 1 mΩ, life cycle >1 million cycles, and support for 10-minute fast charging.
A single module supports 15-21 kW power output, matching the GB300's peak power consumption. With a cycle life > 1 million cycles, it ensures operation > 6 years.



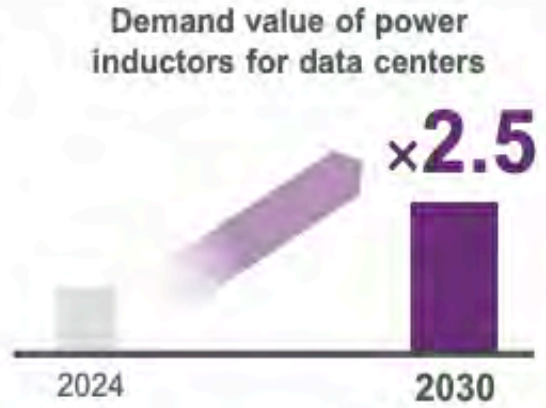
https://passive-components.eu/nvidia-gb300-boost-hybrid-supercapacitor-demand/
https://www.eetimes.com/five-innovative-practices-for-capacitors-in-the-era-of-third-generation-semiconductors/#genecy-interstitial-ad

https://passive-components.eu/skeleton-releases-graphenegpu-to-reduce-ai-energy-consumption-by-44-and-boosts-power-by-40/

Inductors

AI Server power consumption rapidly rise
Optimizing power efficiency contributes to power saving

Inductor Requirements



Higher Current Handling

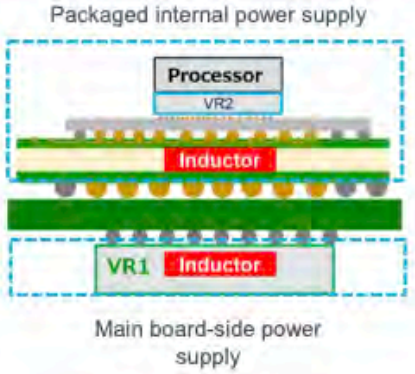
high-performance GPUs / AI accelerators running in **high-current environments**
Inductors must have **higher saturation current** to avoid overheating, functional failure, or damage

Greater Power Density

Data centers face **space limits** and **heat dissipation challenges**
Inductors need **compact form factors** with **low DC resistance (DCR)** to cut thermal losses and boost efficiency

High-Frequency Performance

Next-gen **high-frequency DC-DC converters** demand inductors with **excellent high-frequency characteristics** for stable, efficient power delivery



Thermal Stability & Reliability

AI servers run at **sustained high loads** in **harsh thermal environments**
Inductors must maintain **performance over time** without degradation

Material Innovations

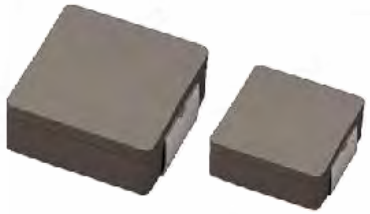
New **nanocrystalline alloys** (e.g., Fe-B-P-Cu) deliver **high magnetic flux density** and **low coercivity**, enabling **smaller, more efficient inductors** for AI workloads

Images source: Murata

Inductors

High Saturation Inductors

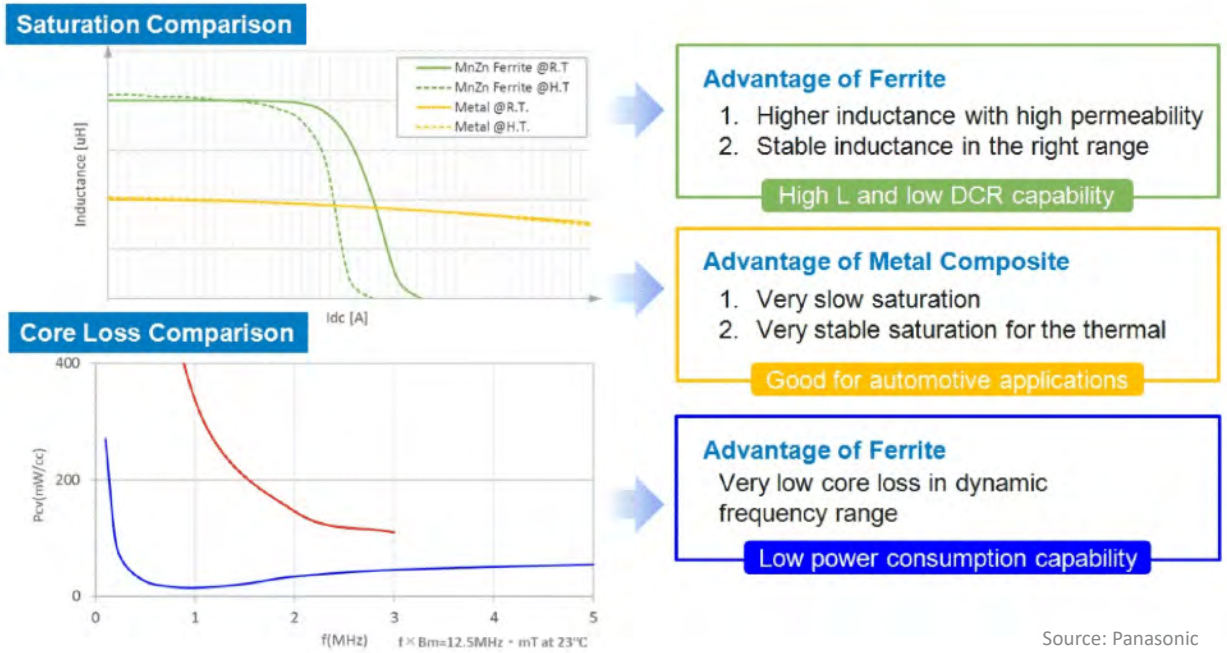
New nanocrystal metal composite magnetic materials featuring high saturation, temp stability





Flat Wire Inductors

Flat wire MnZn ferrite core construction increases saturation currents up to 25% at low core losses



Source: Panasonic

Inductor Technology	Inductance	Magnetic Saturation	Thermal TC	Efficiency	DCR	Insulation Resistance to Core
Metal Composite	Low	Very Good (Soft)	Verry Good	Good	Low to Medium	Good
Ferrite (Mn-Zn)	High	Not as Good (Hard)	Not as Good	Very Good	Low	Not as Good
Ferrite (Ni-Zn)	Medium	Good (Hard)	Good	Good	Lot to High	Very Good

Source: KEMET YAGEO

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Inductors

One Turn Inductors

One-turn Mn-Zn ferrite inductor minimizes heat generation and energy loss, supporting switching frequencies up to 3 MHz

DC Optimization:

hard-switching applications (multi-phase buck converters)
reduced DCR to minimize copper losses, enhancing system efficiency

AC Optimization

soft-switching architectures such (STC Switched Tank Converters)
ferrite core with precisely engineered air gap reduce AC losses caused by eddy currents and fringing flux

Low Loss Inductors

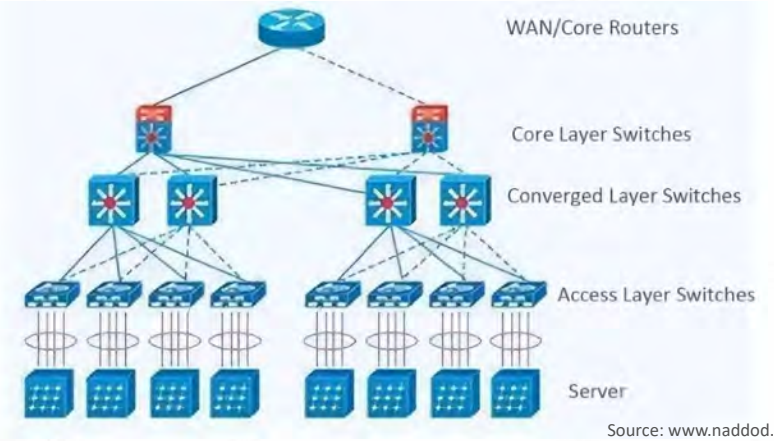


AI adoption drive demand for high-speed and high-capacity data transfer communication within a Whole Communication Chain

High frequency, Low loss solutions and components

Components for Optical Transceivers

Critical Role in AI Workloads – Optical transceivers enable ultra-fast, high-volume data exchange across AI compute nodes.
High-Speed Links – Power 400G/800G+ connections for GPU-to-GPU, node-to-node, and rack-to-spine traffic.
Data-Center Backbone – Support low-latency interconnects between servers, storage, and network switches.
Scalable Infrastructure – Handle growing AI cluster sizes where copper cabling can't meet bandwidth or distance needs.
Long-Haul Performance – Coherent optics connect AI facilities across campuses or regions without throttling throughput.



Source: www.naddod.com

Latest Inductor example targeting optical transceivers:

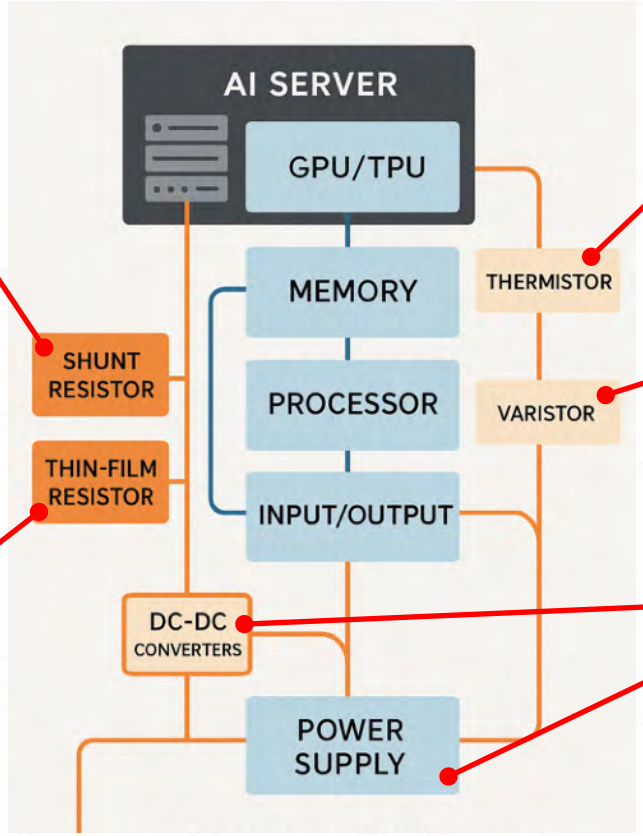
thin-film chip inductor 1.2 x 0.6 x 0.95 mm
DC resistance reduced by 70%,
Rated saturation current increased by 1.7 times

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Resistors

Resistors in AI Servers

Current-sense resistors in hot-swap circuits and DC-DC converters must handle **higher continuous currents** and **steeper slew rates** without drifting, so low-ohmic, high-power shunt designs with excellent thermal stability are in demand



Thermistors (NTC/PTC) are critical for inrush current limiting and temperature monitoring in dense AI racks.

Varistors (MOVs) protect against voltage surges from grid fluctuations or lightning — a bigger concern as AI data centers scale power delivery

Thin-film SMD chip resistors in 0402/0201 with **higher pulse-handling** and **better heat dissipation** to fit into compact accelerator boards without sacrificing reliability

Move toward **wide-bandgap power devices** (SiC, GaN) in AI server PSUs changes switching speeds and EMI profiles, which in turn drives demand for resistors with **low parasitic inductance** and stable high-frequency performance

Resistors

The Resistor Becomes a Measurement Instrument for AI Environment

Current sensing moved from niche specialty to volume strategic segment at 8–14 % CAGR

AI datacentre function	Specification	Cost vs commodity
PDU telemetry	1–5 mΩ through-hole, 25–100 W	15–25×
Instrumentation-amp feedback	10–100 kΩ, ±0.1–0.5 %, <25 ppm/°C matched	4–6×
GPU/CPU VRM phase sensing	0.5–5 mΩ Kelvin, ±0.5–1 %, <50 ppm/°C, 2–3 W	3–5×
48 V bus monitoring	0.5–2 mΩ, 3–5 W	3–4×
VRM feedback divider	10–100 kΩ thin film	2–3×
Gate drive / pull-up	5–47 Ω thick film ±5 %, pulse >10×	baseline

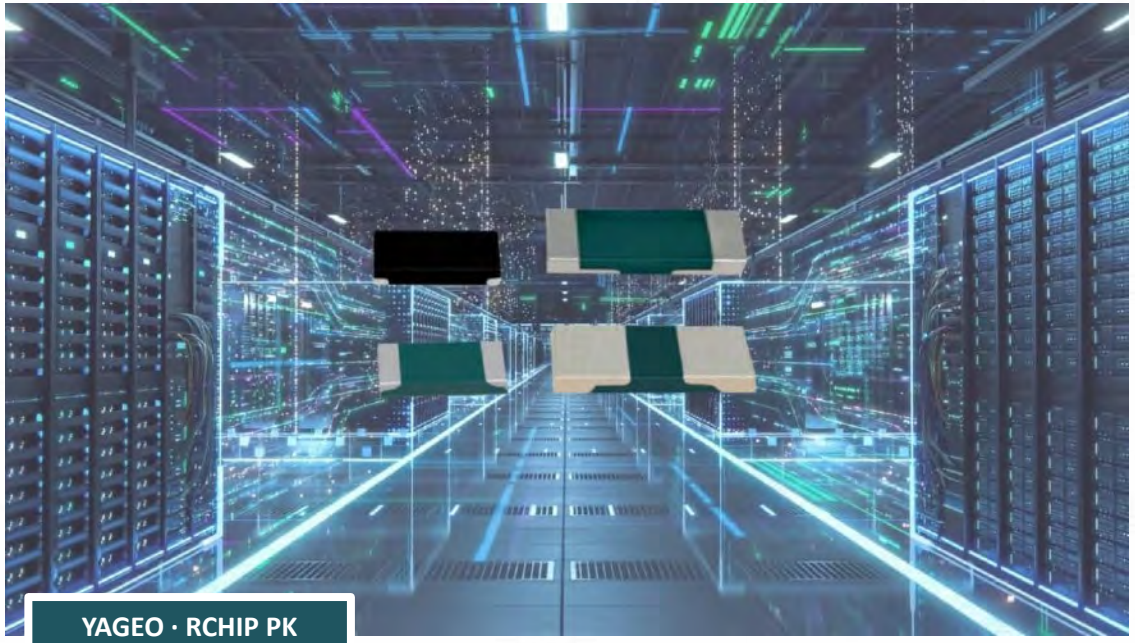


- **Only 5–6 suppliers hold production-scale ±0.5–1 %, <50 ppm/°C Kelvin capability**
- **15–30 current-sense resistors sit in every 8-GPU server.**

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Demonstrator: Current Sensing and HV Protection

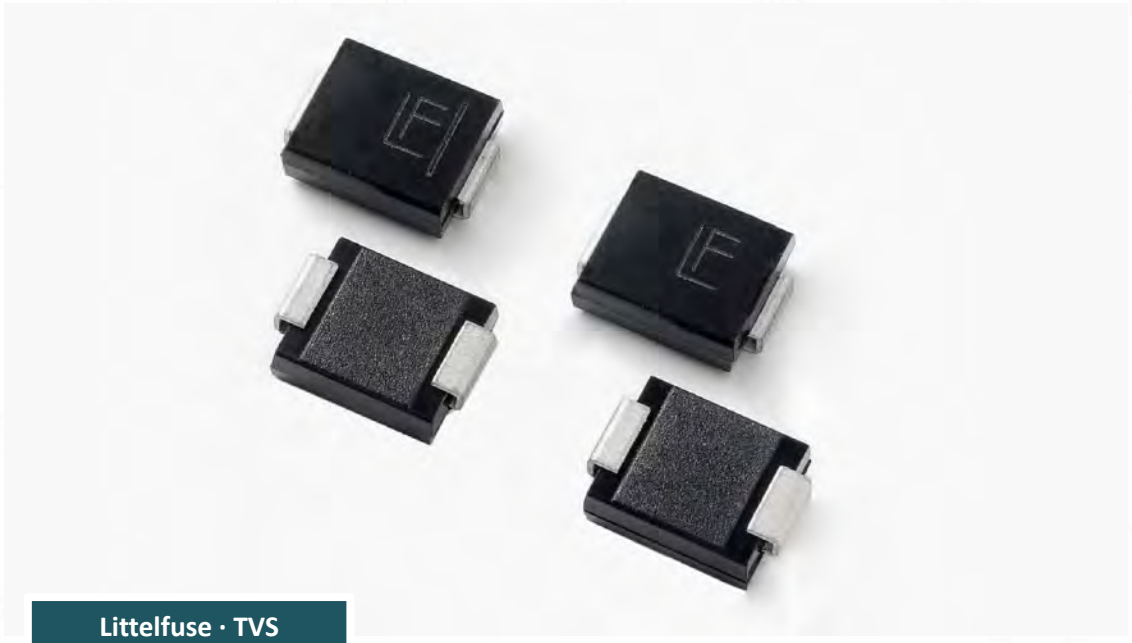
Metal shunts to 170 °C and single-device TVS to 540 V



YAGEO · RCHIP PK

PK metal current sensors, 1206 and 2512

- **0.5–20 mΩ** resistance range; 50 or 100 ppm/°C
- **2–5 W** power rating; maximum surface temperature 100 °C
- **–55…+170 °C** operating range
- **AEC-Q200** qualified — AI servers, BMS, inverters



Littelfuse · TVS

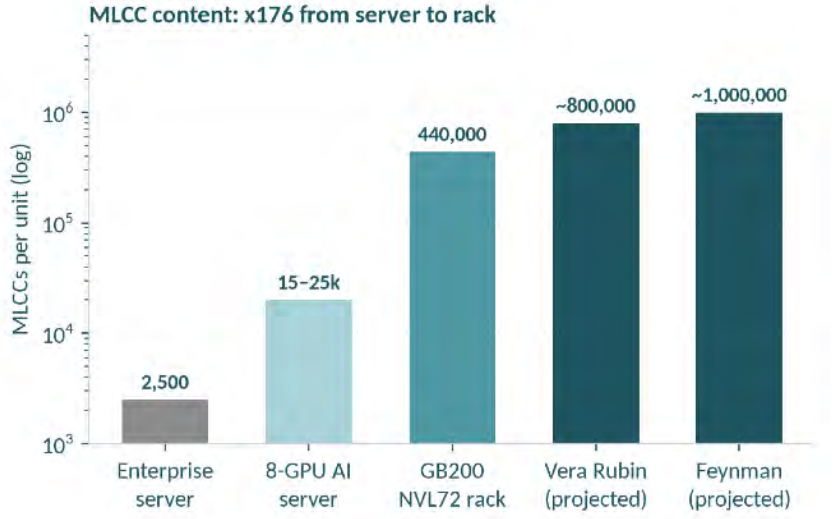
TPSMC, TPSMD and TP5.0SMDJ high-voltage TVS

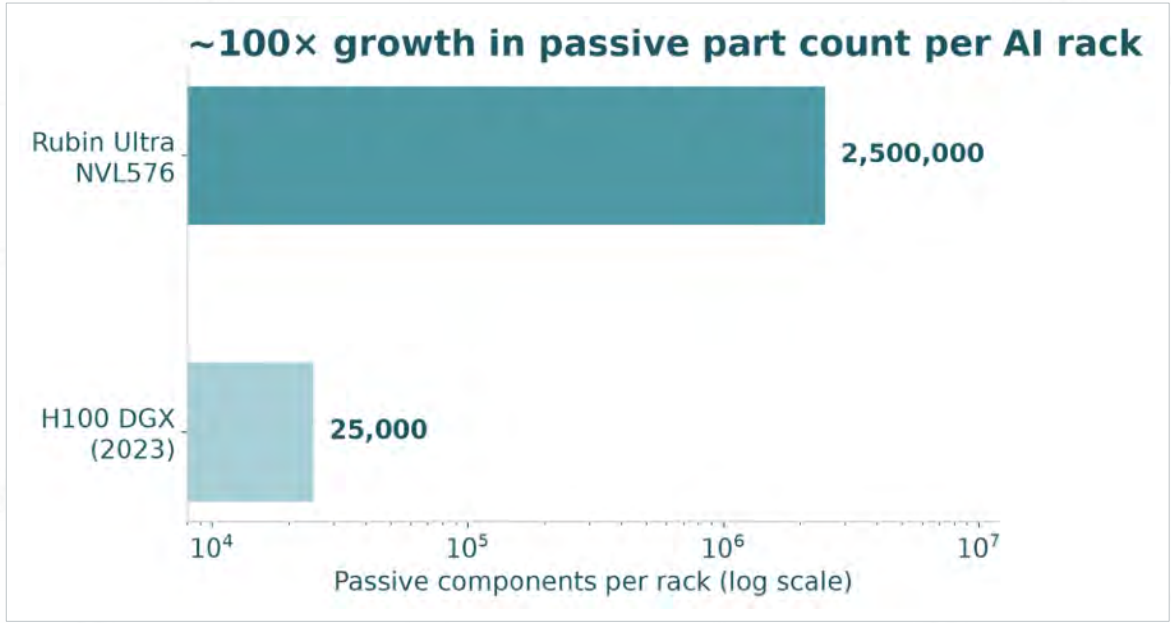
- **300–540 V** TPSMC stand-off at 1,500 W; TPSMD 180–400 V at 3,000 W
- **5,000 W** TP5.0SMDJ peak pulse power at 10/1000 µs
- **< 1 ps** response; up to 300 A surge; ESD to 30 kV
- **DO-214AB** SMC package; leakage < 1 µA above 13 V

Source: YAGEO PK | Littelfuse high-voltage TVS

AI Power Management - Passive Part Count

MLCC content per unit grows faster than compute itself





> 2,500 A

Current at 120 kW on a 48 V bus (GB200 NVL72)

< 0.5 mΩ

DCR now demanded of AI-server power inductors

180–250

Magnetic components in a single 8-GPU server

One accelerator platform went from 1,440 to 10,544 capacitors (+632 %). About 3,000 HiCV MLCCs sit on a single GPU board and AI servers carry up to 8× the MLCC content of a conventional server. Hyperscaler commitments of 150,000–200,000 GPU servers per year for 2025–2027 have already absorbed 55–65 % of qualified precision shunt resistors capacity.

"AI MLCC's Law"

The MLCC capacitance required per GPU doubles every year. *Samsung Electro-Mechanics, Sep 2026*

Capacitance value extension by new technologies does not meet the GPU increase of requirements = more capacitor units are needed

Passive Value per Rack Nearly Triples

MLCCs become the third-largest AI-server BOM item after GPUs and memory

GB300 NVL72
USD 1,530

MLCC value per rack, earlier system.

VERA RUBIN NVL72
USD 4,320

MLCC value per rack — +182 %.

AI-SERVER MLCC
USD 1.4 → 5.8 bn

2025 to 2030 market for the grade.

Why: 48 V distribution, near-chip and in-package regulation and high-frequency VRMs raise both counts and specifications.

Next: Vera Rubin local decoupling may need higher-voltage, fine-pitch MLCC down to 0201 or smaller; 20-week-plus lead times through 2027.

Source: Nvidia Vera Rubin: Why One AI Rack Needs More MLCC | EPCI Capacitors Technology Dossier 9/26

Physical AI

AI systems that operate inside physical machines — sensing, interpreting, and acting on real-world data in real time, directly at the point of action.

Cloud AI

- Centralized data center processing
- High latency — round-trip to cloud
- Requires constant connectivity

Physical AI

- Local edge/far-edge processing
- Near-zero latency — on-device
- Operates autonomously offline

01

Mainframe Era

Centralized compute in large systems. All processing happens in one location.

02

Cloud AI Era

AI models trained and run in hyperscale data centers. Requires network connectivity.

03

Physical AI Era

AI moves to the edge. Models run locally inside machines that sense, interpret, and act.

Physical AI - Nvidia Physical AI HW 2026 Offering

Local Agentic AI: Personal, Private and Fast

The three hardware layers

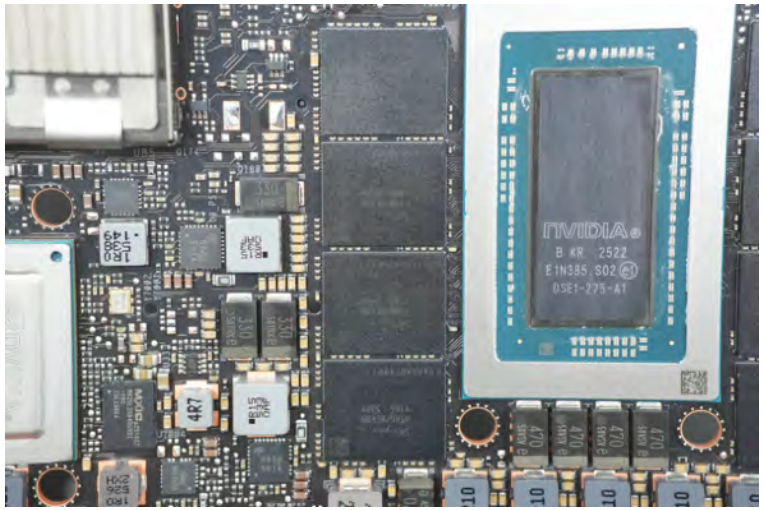
Physical-AI stage	NVIDIA hardware	Primary job	Typical deployment
Model training	NVIDIA DGX systems	Train or fine-tune large vision-language-action, perception, and robotics foundation models	AI factory / data center
Simulation and synthetic data	RTX PRO Servers running Omniverse and Cosmos	Simulate robots, sensors, factories, and edge cases; generate synthetic data; test policies before physical deployment	Data center / private cloud
Real-time edge inference	Jetson AGX Thor	Processes cameras and other sensors, runs perception/reasoning/control models, and produces low-latency robot actions	Inside robot, autonomous machine, or smart-space controller

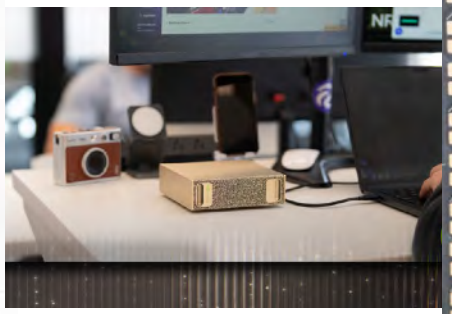
A simplified selection rule:

Requirement	Likely platform direction
Prototype vision robot or smaller embedded AI system	Jetson family
High-performance robot with VLA/reasoning models	Jetson AGX Thor
Industrial/medical equipment needing functional-safety architecture	IGX Thor
Autonomous vehicle platform	DRIVE AGX Thor
Training world/foundation/robotics models	DGX
Digital twin, sensor simulation, synthetic data at scale	RTX PRO Server

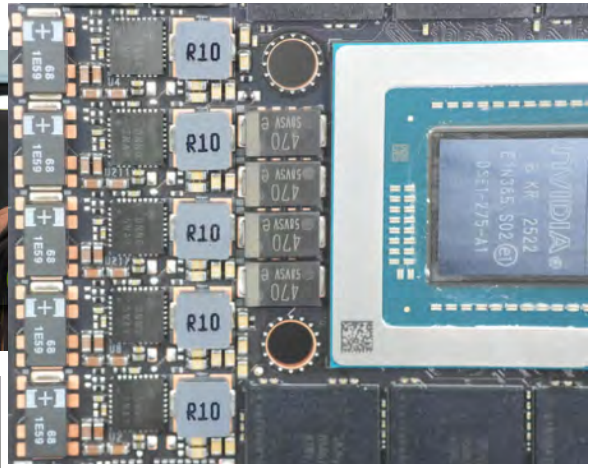
Lightweight AI server NVIDIA DGX Spark

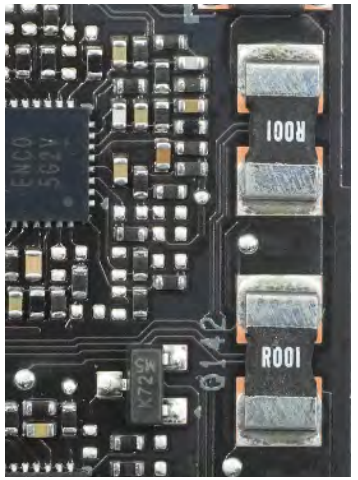
- **Processor:** NVIDIA GB10
  - Grace Blackwell Superchip
- **CPU:** 20 cores
- **GPU:** 6,144 CUDA cores;
  - **1 PFLOPS FP4** AI performance
- **Memory:** 128 GB
- **Storage:** 4 TB
- **GB10 TDP:** 140 W
- **Dimensions:** 150 × 150 × 51.2 mm
- **Weight:** Approx. 1.25 kg











- Tantalum polymer input capacitors 68µF 25V (12V line)
- Alum SMD polymer output filter capacitors 470µF 2.5V
- 0.1µH buck inductors
- two 1mΩ resistors are used for current detection

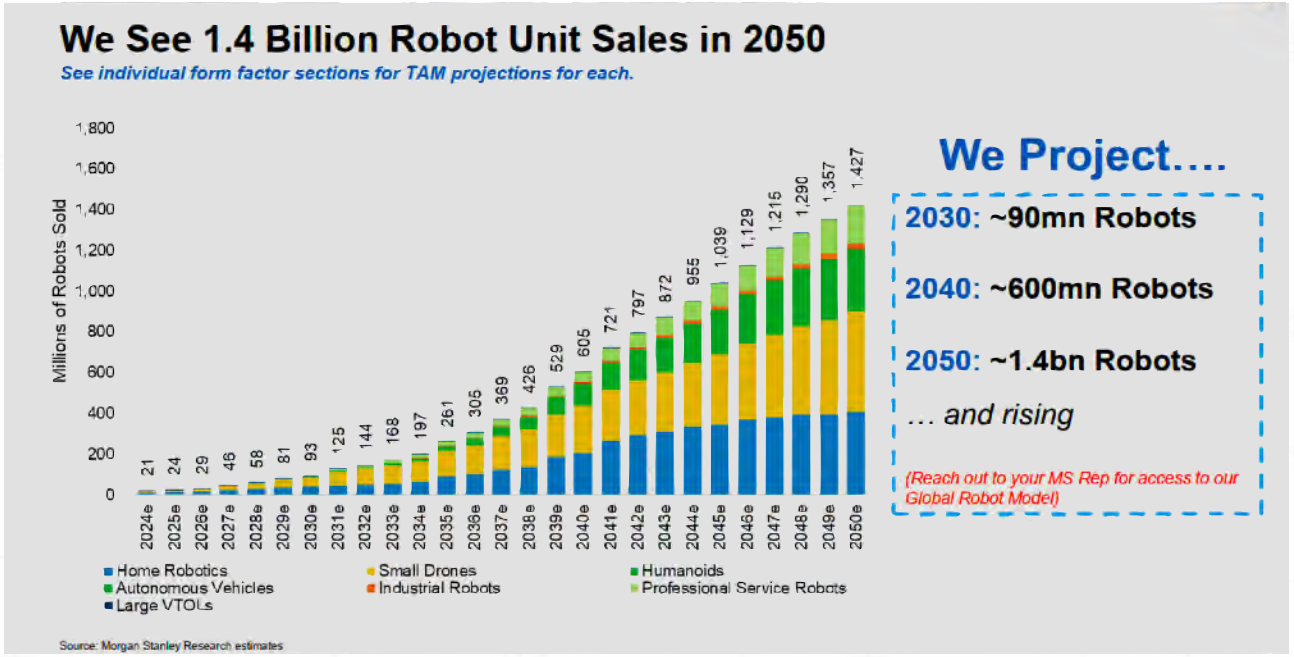
Source: https://www.chargerlab.com/teardown-of-nvidia-dgx-spark-4tb

Physical AI - Robotics

Industrial robotics is currently one of the fastest-moving sectors adopting physical AI

"The robot needs to be able to act immediately based on perception, sensing, touching, and vision. If it has to send information to a data center and wait for an answer, the robot will be useless."

— Gilles Garcia, AMD



"I believe that in the next ten years humanoid robotics could become one of the biggest transformations to support people." — Gilles Garcia, AMD

Manufacturing **Healthcare Assistance**
Elderly Care

Unit	Chip / Platform	CPU Cores	TDP	Key Workloads
CPU	Ryzen Embedded 9000 (Zen 5)	6 – 16 cores 12 – 32 threads	65 – 170 W	Sequential logic, control systems, OS orchestration
GPU	Integrated RDNA 3.5	Up to 8 WGPs (16 CUs)	Shared w/ SoC TDP	Machine vision, image processing, parallel inference
NPU	Ryzen AI P100 (XDNA 2)	4 – 12 cores (SoC: Zen 5/5c)	15 – 54 W (SoC TDP)	Neural network inference, sensor fusion, classification

Small Robots / Edge Sensors 5 – 15 W

Robotic Platforms 10 – 50 W

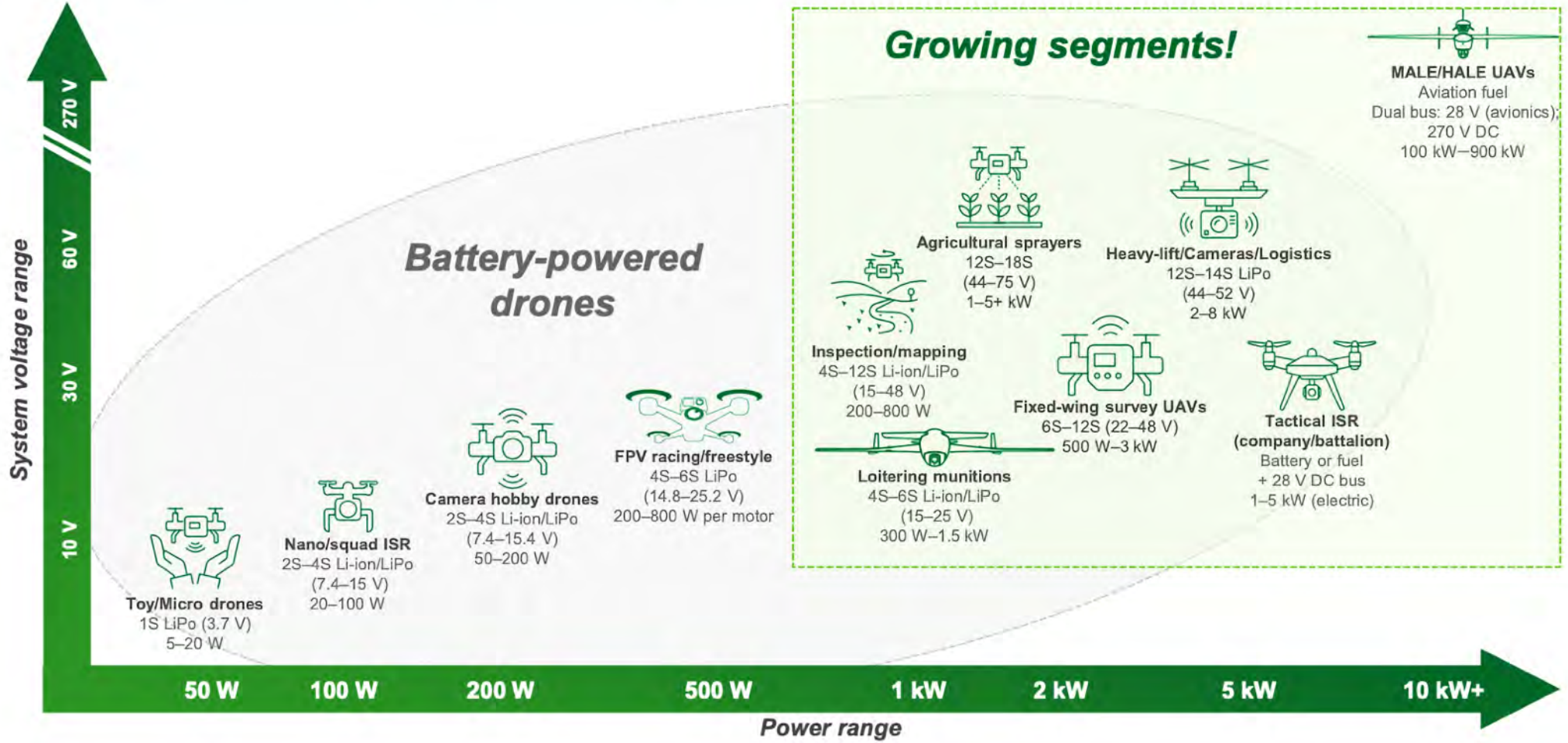
Industrial PCs (Ryzen 9000) 65 – 170 W

Source: AMD, AInvest, Deloitte, Morgan Stanley

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Physical AI - Robotics

Drone & UAV Market Shift Towards Commercial & Defense Applications



Source: Littelfuse

Physical AI: AI Leaves the Data Centre

Edge compute, actuation and sensing in machines that move

Edge compute

Same PDN problem at lower power: 0.6–1.2 V core rails and 1.8–5 V auxiliary rails on SoC, GPU and NPU modules.

Actuation

Motor drives on 48 V robot buses and 400–800 V industrial DC links; decentralized conversion moves into joints and limbs.

Sensing

Vision, IMU, tactile and force sensors with high-resolution ADC front ends need low-noise, stable decoupling.

Power density: components supporting up to 40 MHz switching allow power stages directly above or below chips.

Europe: Würth argues Europe's physical hardware and power infrastructure may be the primary constraint on AI scaling.

Source: Every Watt Counts | Samsung MLCC guide for robots | EPCI Industrial & Robotics Dossier

Industrial and Robotics: 24 V → 48 V → 800 V DC

Factory electrification and humanoids create a new high-density passive class

INSTALLATIONS 2024

542,076

industrial robots; operational stock 4.66 million.

HUMANOID

~240 MOSFETs

and 280–300 switch positions per 40-joint platform.

SWITCHING

→ 1 MHz

SiC and GaN in drives; > 60 % core-loss cut ferrite → nanocrystalline.

SPE

10 Mb/s, 1,000 m

10BASE-T1L in-robot links; PoDL changes the EMC budget.

THE TWO-SPEED MARKET

Commodity back, specialist tail stretched

Commodity MLCC back to 8–18 weeks.

DC-link film 20–40 wk; tantalum polymer 22–32 wk; pyrotechnic fuses 20–36 wk; large-can electrolytics 30–52+ wk.

AI-data-centre demand is outbidding industrial buyers for the same capacity.

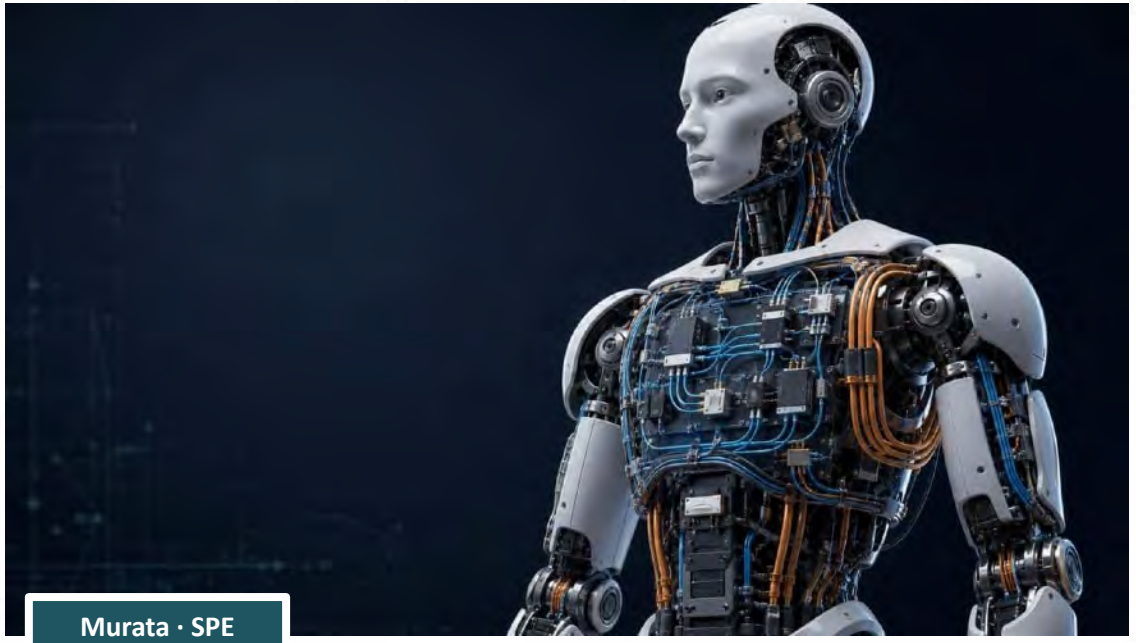
Source: EPCI Industrial & Robotics Dossier | EPCI Technology Dossiers 2026

Demonstrators: Inside a Humanoid Robot

MLCC selection and single-pair Ethernet in robot joints



Samsung EM · Robotics



Murata · SPE

MLCC selection guide for humanoids and robots

- **47 µF 0402 X6S** for AI compute rails; 330 µF 1210 for transient bulk
- **10 µF / 100 V X7S** 1210 with soft termination, 5 mm bend, for 48 V actuators
- **4.7 µF / 125 V X7T** 1210 for DC-link and snubber duty
- **Flex robustness** listed alongside capacitance as a selection parameter

Single-pair Ethernet for in-robot networks

- **50–80 actuators** per humanoid; up to 72+ degrees of freedom
- **Up to 300 Nm** joint torque; payload ambitions above 25 kg
- **10 Mb/s–1 Gb/s** 10BASE-T1S, 100BASE-T1, 1000BASE-T1 PHY options
- **≈ 52 W** PoDL at the power sourcing equipment; SCH1633-D05 6DoF IMU

Source: Samsung MLCC guide for robots | Single-pair Ethernet for humanoids

Anatomy of an Autonomous Platform

Every block carries its own passive bottleneck

Battery / HV source
Supercap or hybrid buffer, pyro fuse

→

HV DC bus 48–800 V
DC-link film, TVS, ≥ 1,200 V rating

→

Inverter + motor
SiC/GaN, CMC, snubber C0G, shunt

→

Actuators / propulsion
Encoders, braking resistors

AI compute module
X6S high-CV MLCC, TLVR, silicon C

Sensors
Low-noise MLCC, thin-film R, ESD

RF / data link
50 GHz thin film, C0G, filters

Protection & safety
SSPC, fuses, functional safety

Low-voltage DC-DC from the HV bus feeds the lower row; EMC filtering links both rows.

Source: Exxelia 1200 V for 800 V aerospace | Littelfuse AK-FL | Vishay CHEP | Samsung MLCC guide

Drones and UAVs: SWaP Meets Physical AI

The autonomy stack in its most compressed form

Compute

Edge-AI modules reuse X6S high-CV MLCC and fast VRM magnetics from the data-centre PDN.

Propulsion

High-power drones listed among 800 V aerospace targets for 1,200 V film and integrated magnetics.

RF and guidance

Thin-film AlN resistors to 50 GHz named for drone communications, guidance, phased-array radar.

Protection

HV TVS, CMC chokes for GaN/SiC dv/dt, and EMC filtering in tight volumes.

DUAL-USE REALITY

The same component families serve commercial drones and defense platforms — screening level, traceability and export status decide the version, not the technology.

Source: Exxelia 1200 V for 800 V aerospace | Vishay CHEP 50 GHz | Vishay SGCM05339 | EPCI AI Hardware Dossier

800 V HVDC Enters the Data Centre

Grid-to-rack conversion brings EV and defense / aviation-class passives inside

13.8 kV AC grid
MV feed

→

SST front end
2.3–6.5 kV SiC, cascaded H-bridge

→

800 V DC bus
DC-link, protection, SSCB

→

Rack DC-DC
1.2–2.3 kV SiC, LLC/ CLLC

→

48 V → core
TLVR, MLCC, silicon

Capacitors

DC-link sized for startup, load rejection, faults and transients; C0G/ KC-Link to 3 kV for resonant tanks and snubbers; ≥ 1,000 V-class parts reused from EV.

Magnetics

HF isolation transformers, resonant and boost inductors, DM/CM chokes; core loss under real waveforms, partial discharge, creepage.

Why 800 V

157 % more power than 415 VAC on the same conductor gauge; NVIDIA announced 800 V HVDC distribution from 2027.

Source: SSTs for 800 V AI Data Centers | C0G HV MLCC for 800 V AI | EPCI Capacitors Technology Dossier 9/26

Two AI Worlds, Two Sets of Passive Priorities

AI cloud pushes density and volume; physical AI pushes robustness

Dimension	AI cloud (data centre)	Physical AI (robots, vehicles, aircraft)	Space / defence extension
Power level	Kilowatt-class GPU packages; > 100 kW racks	Watts to tens of kW per platform	SWaP-limited, radiation
Bus voltage	48/54 V → 800 V HVDC from 2027	24 → 48 V robot bus; 270–800 V aviation	28 V / 100 V / HV PPU
Environment	Controlled, liquid-cooled	Vibration, shock, −40…+125 °C	Vacuum, −55…+125 °C, TID
Binding passive metric	ESL, effective C, DCR, part count	Flex robustness, surge, EMC, safety	Screening, traceability, derating
Qualification	Hyperscaler validation, volume LTAs	AEC-Q200, IEC 61508, ISO 13849, DO-160	MIL-PRF, ESCC, EEE-INST-002

The technology flows from the cloud column outward; the qualification evidence must be rebuilt for every column to its right.

Source: EPCI AI Hardware Dossier | EPCI Industrial & Robotics Dossier | Exxelia 1200 V for 800 V aerospace | Littelfuse AK-FL

What Transfers From AI Hardware to Space

Technology is ready earlier than the qualification evidence

AI-driven technology	Space value	Evidence available	Gap to close
High-CV X6S / X7R MLCC	Mass and area per µF	HRA X/Z screening	Effective-C data
Polymer tantalum (automotive)	Low-ESR bulk for PoL	10,000 h; 212 krad (T598)	ACC in vacuum; 50 % derating
Silicon trench capacitors	Rad-hard, −250…+300 °C	293 krad; TDDB > 50 y	AEC / ESCC family, MSL
1,200 V film, C0G HV	800 V-class PPU, EP	Aviation AS9100 lines	Outgassing
Nanocrystalline CMC, TLVR	GaN / SiC converters	EEE-INST-002 screening	Radiation data per P/N
AlN thin-film resistors	RF and precision power	To 50–70 GHz	Pulse, space life data
Supercapacitors	Pulse loads, launchers	32 FIT, 11,000 h vacuum	Temperature limit

Source: EPCI Aerospace & Defence Dossier 9/26 | KEMET HRA | T598 LEO | Silicon capacitors | Vishay SGCM05339

Defense Demand Becomes Visible in the Data

Rising budgets and modernization programs add to the AI-driven cycle

CONNECTOR BACKLOG
USD 34.3 bn

June 2026, up from USD 24.1 bn — AI and defence named as drivers.

EUROPE BOOKINGS
+28.9 %

year-to-date bookings growth to June 2026.

BOOK-TO-BILL
1.07

June 2026 vs 1.00 for full-year 2025.

BACKLOG COVER
14.7 weeks

end of June 2026 vs 12.6 weeks at end 2025.

Paumanok view: LEO constellations, launch activity and government investment expand demand for space-qualified capacitors and resistors.

Implication: hi-rel lines see rising demand at the same time as AI absorbs high-end commercial capacity and materials.

Source: Connector Industry Performance mid-2026 | Advanced Electronics Markets Reshape Capacitor Demand

Hi-Rel Supply Base and Sovereignty

Consolidation, ITAR-free options and ring-fenced material chains

Consolidation

Evans Group unified Evans (hybrid wet tantalum), Paktron (polymer film), UTC (hi-rel MLCC, MIL-PRF-39014 / 55681) and Eulex (RF ceramic) — all US-based.

Dual-region production

Exxelia offers 1,200 V film and magnetics from Europe and the USA, with ITAR-free options and a no-obsolescence policy.

Material ring-fencing

Murata is separating China-related rare-earth supply from its global chain over about three years.

FOR EUROPEAN SPACE

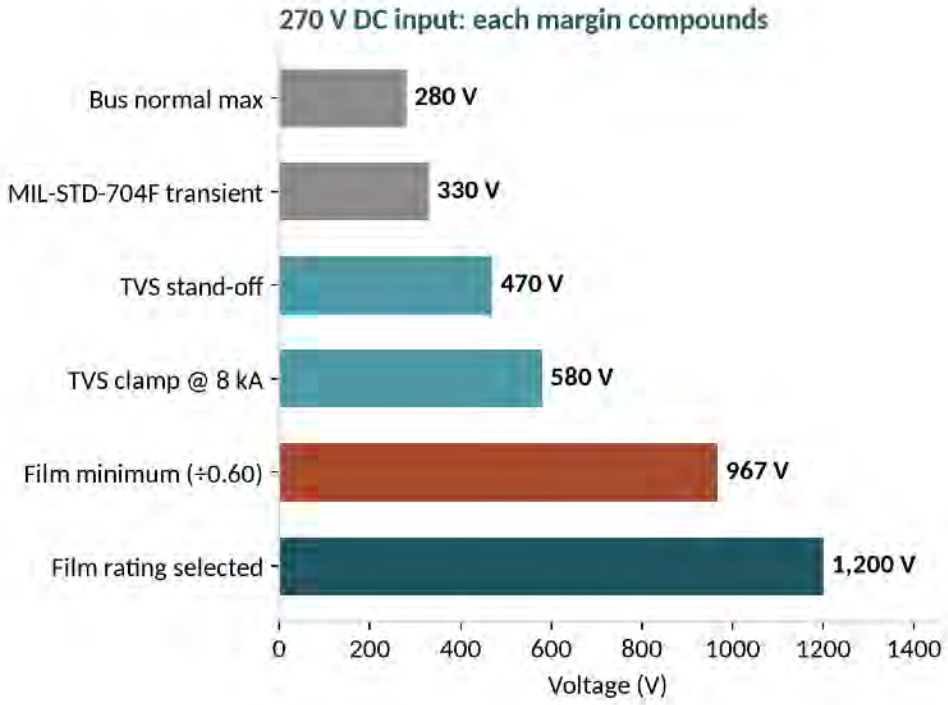
Non-dependence is a supply-chain design choice made at qualification time: where the powder, paste, film and line sit matters as much as the part number.

Source: Evans Group | Exxelia 1200 V | Murata rare earth decoupling

Worked Example: Airborne 270 V DC Input

MIL-STD-704F transients drive TVS, film rating and hold-up

Design step	Value	How it follows
Normal range / transients	250–280 V; +330 V / −200 V	MIL-STD-704F
TVS (AK8-470C-FL)	470 V stand-off, 580 V clamp at 8 kA	42 % margin over 330 V
Film rating needed	≥ 967 V	580 V ÷ 0.60 derating
Film available (CF-PP140)	450–1,500 V, 140 °C continuous	Select ≥ 1,000 V class
Hold-up energy	25 J	500 W × 0.050 s
Hold-up capacitance	1.30 mF	280 V → 200 V discharge
Overcurrent	USE 2410-class fuse, 200 A breaking	AEC-Q200 tested



Check: C = 2 × 25 J ÷ (280² − 200²) V² = 1.30 mF. Each design is limited by derating and system transients, not nominal ratings.

Source: EPCI Aerospace & Defence Dossier 9/26 | Littelfuse AK-FL | Exxelia 1200 V film

Demonstrators: Film and Magnetics Proven in Flight

From BepiColombo to GaN-ready space EMI filters



Exxelia · BepiColombo

Film capacitors, CMC chokes and inductors en route to Mercury

- **PM90X film** 50–1,250 V DC, −55…+125 °C, self-healing
- **CMC chokes** 50 µH–4.9 mH to 14.3 A; ESCC 3201/010 on request
- **SESI inductors** 1 µH–6.8 mH, 24 A, smoothing to 1 MHz



Vishay · SGCM05339

Space-grade SMT common-mode choke for GaN / SiC

- **320–10,400 µH** 2.02–14.43 A, −55…+130 °C
- **EEE-INST-002** and MIL-STD-981 Class S/B screening
- **8–12 weeks** lead time

Source: Exxelia BepiColombo | Vishay SGCM05339

Six Points to Take Back

1. **AI power delivery is the demand engine**. Target roadmap against 120 kW racks today and megawatt roadmaps, not yesterday's 10–20 kW.

2. **Parasitics are the binding constraint.** ESL, DCR and mounting inductance now decide feasibility; capacitance and inductance no longer do.

3. **Everything above ~200 MHz moves into the package**. Land-side, die-side, interposer and on-die tiers are production reality, not research.

4. **Wide-bandgap transfers the engineering burden to the passive**. Above ~300 kHz, core material, thermal design and protection speed become the limits.

5. **Value has already left the commodity part.** ~40 % of value and 60–72 % of profit sit in strategic segments .

6. **Qualify in 2026 to ship in 2028.** With 12–18 month line qualifications and capacity pre-sold, sourcing is a design-phase decision.

THE STRUCTURAL SHIFT

Passive components have moved from the last line of the BOM to the first constraint on system performance.

Value is migrating away from commodity parts: strategic segments are ~40 % of market value but 60–72 % of operating profit in capacitors, magnetics and resistors.

Source: EPCI Technology Dossiers 2026 — passive-components.eu

Ten Takeaways for the Space Passive Community

From the AI upcycle to the next qualification cycle

1. AI is the demand engine; passives are its first physical constraint.
2. The shortage is grade-specific; hi-rel shares plants and materials with it.
3. 2026 broke price discipline — cumulative MLCC +15–40 %, tantalum ×2.6.
4. Design to effective values: 10 µF in 0402 keeps 16 % at 5 V.
5. Above ~100 MHz, mounted inductance decides; capacitance moves into the package.
6. 800 V spreads from EV to data centre to aviation: ≥ 1,200 V parts and fast TVS.
7. The QPL envelope widens — BME on MIL-PRF-32535, polymer Ta on QPL routes.
8. COTS for LEO works with upscreening, but documentation is the first barrier.
9. Radiation and vacuum data are the gap in most bridge-grade launches.
10. Qualify in 2026 to fly in 2028: sourcing is a design-phase decision.

Source: EPCI Capacitors Technology Dossier 9/26 | EPCI Aerospace & Defence Dossier 9/26 | EPCI Technology Dossiers 2026

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- PASSIVE SENSORS
- INTERCONNECTION
- CRYSTALS & OSCILLATORS

1st Feb 27	Call for papers announcement
1st Apr 27	Abstract deadline
31 Apr 27	Notice of acceptance
1st May 27	Registration opens
7th May 27	Preliminary programme
1st Jun 27	Full Paper deadline
16 July 27	Early registration up to
23 July 27	Final programme
7-10th Sept 27	Conference date

7-10th September 2027

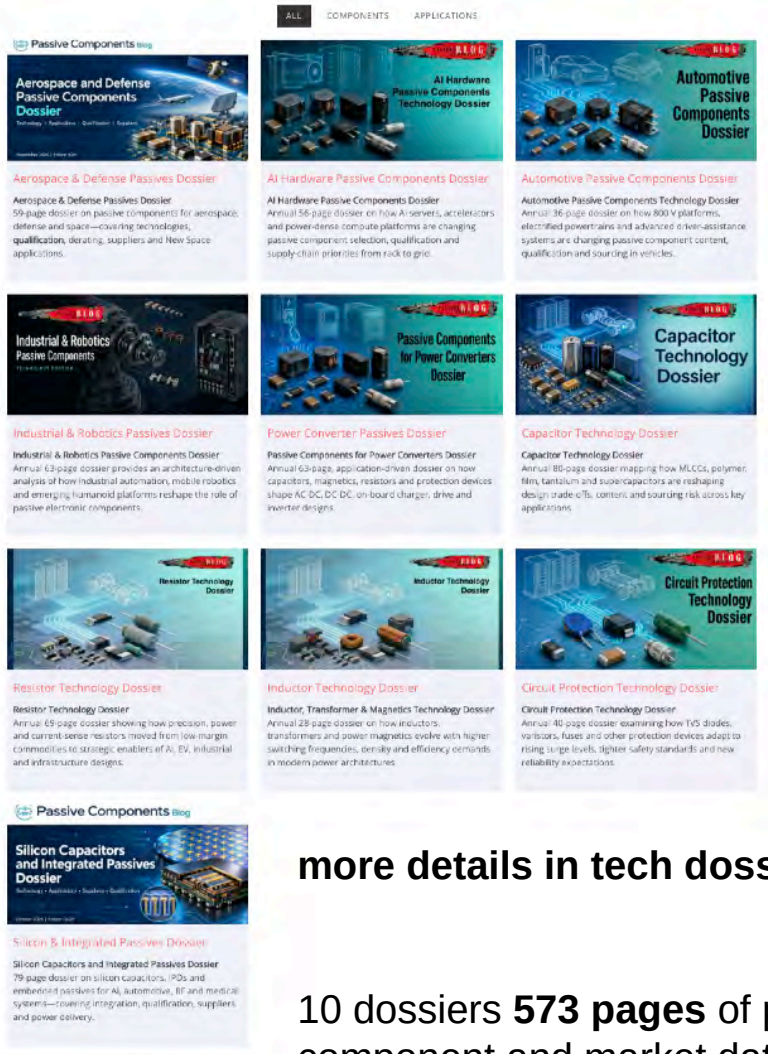
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Theme: Power Electronics

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more details in tech dossiers

10 dossiers **573 pages** of primary component and market data

https://passive-components.eu/technology-dossiers/

Thank You!

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